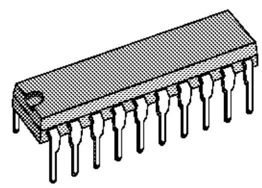
L6223A

DMOS PROGRAMMABLE HIGH SPEED UNIPOLAR STEPPER MOTOR DRIVER

ADVANCE DATA

- HIGH EFFICIENCY UNIPOLAR STEPPER MOTOR DRIVER
- HIGH SPEED UNIPOLAR STEPPER MOTOR DRIVER
- SUPPLY VOLTAGE UP TO 46V
- PHASE CURRENT UP TO 1A
- UP TO 2A/PHASE IN DUAL CONFIGURATION
- PARALLEL CMOS µP INTERFACE FOR FULL/HALF STEP MOTOR ROTATION
- SERIAL INTERFACE FOR 6 BIT PROGRAMMING
- CLOSE/OPEN LOOP, 8 PWM CURRENT LEVELS
- DUAL PWM FREQUENCY SELECTION
- INPUT BIDIRECTIONALLY PROTECTED
- THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



POWERDIP 16+2+2

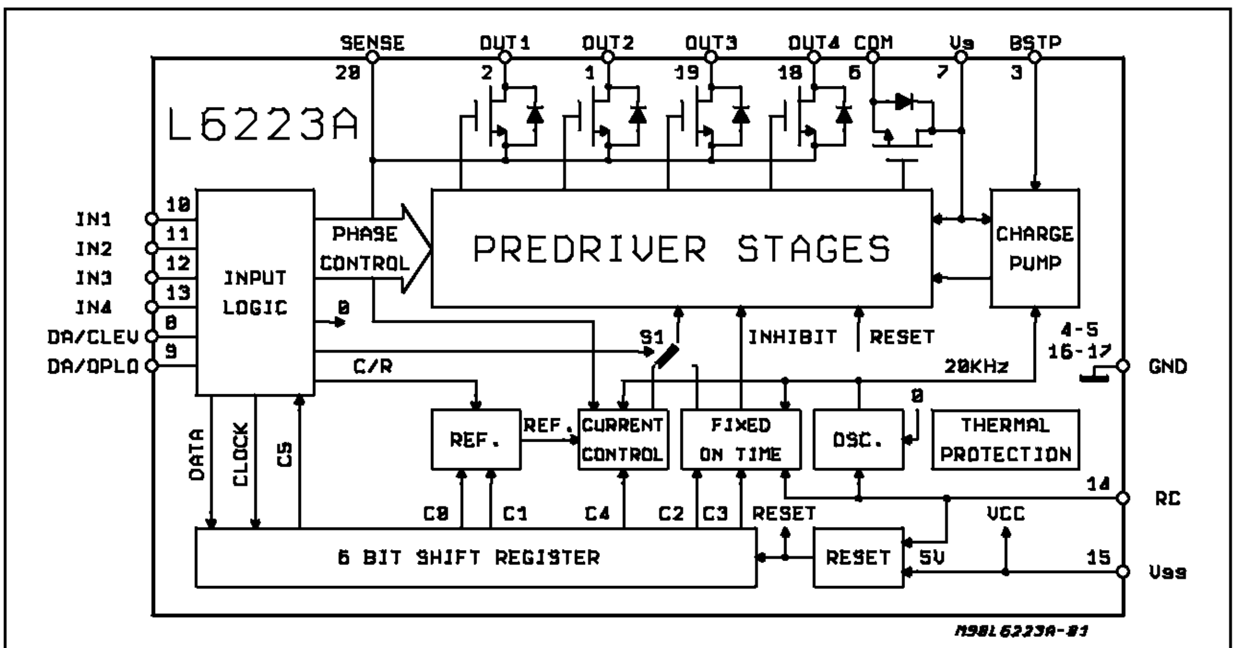
ORDERING NUMBER : L6223A

DESCRIPTION

The L6223A is a programmable integrated system for driving a unipolar stepper motor. It is realized in Multipower BCD technology. The DMOS output stage, realized by a single upper DMOS switch and four lower DMOS, can deliver up to 1A/phase with motor supply voltages up to 46V.

All inputs are CMOS and microprocessor compatible. An internal 6-bit shift register allows the device to be programmed to select different duty cycles in open loop mode and different chopping frequencies in closed loop mode. When the current control is in closed loop mode it is also possible to select a reduced current chopping level to optimize system efficiency. The L6223A is de-

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

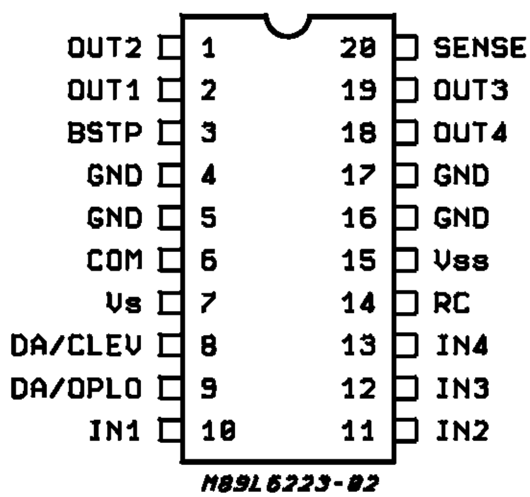
signed to work with a single sense resistor. During chopping t(OFF) time the current is reduced by half, improving efficiency. Higher current applications can be achieved by paralleling two L6223A. The L6223A is mounted in a 20-lead Powerdip package, (16+2+2). Four ground leads conduct heat to dedicated heatsink area on the PCB.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{SS}	Logic supply	7	V
V_S	Supply voltage	50	V
V_I	Logic input voltage (*)	– 0.3V to V_{SS}	
V_O	Output voltage	100	V
V_{Opeak}	Output peak voltage (tpk = 5µs,10% d.c.)	125	V
I_{pl}	Output sink peak current d.c. 10% t(on) = 10µs	3	A
I_{ph}	Output source peak current d.c. 10%,t(on) = 10µs	6	A
P_{tot}	Total power dissipation: T_{pins} = 90°C	4.3	W
	T_{amb} = 70°C (**)	2	W
V_{sense}	Sensing voltage	– 1V to V_{SS}	
T_{stg}, T_j	Storage and junction temperature	– 40 to 150	°C

(*) Oscillator running
(**) 4 cm^2 copper area on PCB, see fig. 34

PIN CONNECTION (top wiew)



THERMAL DATA

$R_{thj-pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	60	°C/W

PIN DESCRIPTION

No.	Name	Function
1,2 18,19	OUT2,OUT1 OUT4,OUT3	Outputs for motor windings.
3	BSTP	A bootstrap capacitor connected between this pin and COM will generate the internal overvoltage required for driving the gate of the upper DMOS.
6	COM	Output for common wire of motor.
4,5 16,17	GND	Common ground. Also provides heatsinking to PCB.
7	V_S	Power supply
8	DA/CLEV	Digital input. 1) In PROGRAM MODE,operates in XOR with DA/OPLO to load data into 6-bit shift register. 2) In OPERATING MODE,works with the other digital inputs to reduce the current level (see Table 2 and Table 3).
9	DA/OPLO	Digital input. 1) In PROGRAM MODE, operates in XOR with DA/CLEV to load data into 6-bit shift register. 2) In OPERATING MODE,selects current control method: open loop (H) or closed loop (L).
10,11 12,13	IN1,IN2 IN3,IN4	Digital inputs. When all inputs are low level,the device is in PROGRAMMING MODE. In OPERATING MODE: 1) FULL MODE - IN1 to IN4 drive the motor phases. A previous programming is requested. 2) SIMPLIFIED MODE - IN1 and IN2 drive the phases,IN3 is ENABLE, IN4 works with DA/CLEV to enable the reduce current level. Previous programming not needed.
14	RC	Input for external RC network. Defines the higher of two possible chopping frequencies. If this pin is set to ground it will reset the IC.
15	V_{SS}	Logic supply.
20	SENSE	Output for sense resistor.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_S = 42V, V_{SS} = 5V, external RC network: R = 18kΩ, C = 3.3nF, unless otherwise specified).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_S	Power Supply		9	32	46	V
V_{SS}	Logic Supply		4.5	5	5.5	V
I_S	Power Supply Quiescent Current	IN1, IN2, IN3, IN4 = L RC = 0V DA/CLEV = L DA/OPLO = L		2	4	mA
I_{SS}	Logic Supply Quiescent Current	IN1, IN2, IN3, IN4 = L RC = 0V DA/CLEV = L DA/OPLO = L		14	20	mA
I_{OL}	Output Leakage Curr.	V_O = 100V (Fig. 1)			1	mA
V_{rs}	Reset Threshold Voltage (Pin 14)				0.9	V
T_{BOOT}	Bootstrap Refresh Pulse	C_{BOOT}= 10nF		3	5	µs

SINK MOS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$R_{DS(ON)}$	ON Resistance	(Fig. 2a and Fig. 3)			1.2	Ω

SOURCE MOS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$R_{DS(ON)}$	ON Resistance	(Fig. 2b and Fig. 3)			0.7	Ω

CURRENT CONTROL SECTION

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{ref}	Internal Reference Volt.	DA/CLEV = L; IN4 = H I_O = 100% nominal value	0.475	0.5	0.525	V
$f_{(OSC)}$	Oscillator Frequency	(Fig. 20)	18	20	22	KHz
$t_{(dis)}$	RC Network Discharge Time (t_{ON} min)	(Fig. 20)	2.3	3	4.3	µs
R_{int}	Internal Discharge Resistor (pin 14)			1.2		kΩ
T_W	Sense Filter Time Constant	(Fig. 4)	1	1.4	2.3	µs

LOGIC LEVELS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(IN)L}$	Input Low Voltage		–0.3		0.8	V
$V_{(IN)H}$	Input High Voltage		2.4		V_{SS}	V

ELECTRICAL CHARACTERISTICS (Continued)

SWITCHING TIMING

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t2, t4	Fall/Rise Time (IN1, 2, 3, 4)	$R_{(load)}$ = 39 Ω (Fig. 5) Pure Resistive Load to V_S			250	ns
t1, t3	Input-Output Delay (IN1, 2, 3, 4)	$R_{(load)}$ = 39 Ω (Fig. 5) Pure Resistive Load to V_S			700	ns
t_{dPWM}	Close Loop PWM Control Delay	(Fig. 4) Note 1			1	µs

PROGRAMMING TIMING

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t1	Loading Time	(Fig. 6)	1.7			µs
t2	Protection Time	(Fig. 6) Note 2	0.2			µs
t3	Data Set-up	(Fig. 6)	0			ns
t4	Data Hold	(Fig. 6)	1.6			µs
t5	Setting Time	(Fig. 6)	200			ns

Note 1) Upper DMOS turn ON delay when the signal is applied at the input comparator (point A in Fig. 4).
Note 2) Internal clock pulse is generated only if IN1...IN4 stay Low for almost 0.2 µs. This delay avoids undesirable programmings.

Figure 1: Output leakage I_{OL} Test Circuit

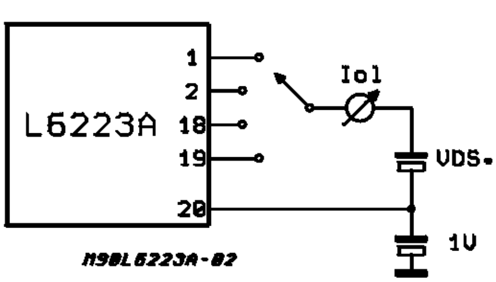


Figure 2a: Source Output DMOS $R_{DS(ON)}$ Test Circuit

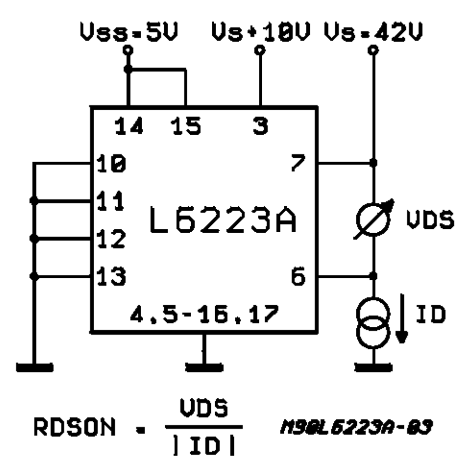


Figure 2b: Sink Output DMOS $R_{DS(ON)}$ Test Circuit

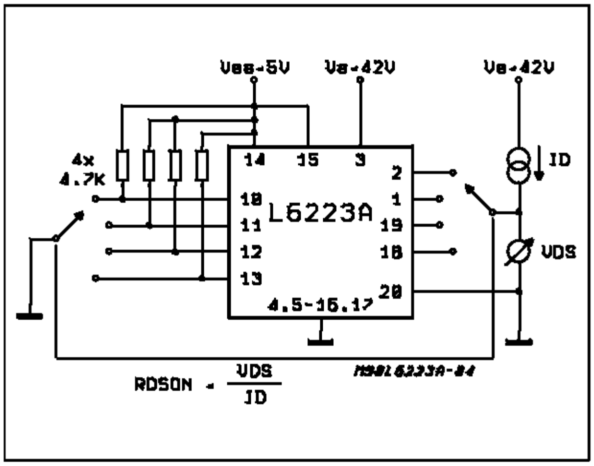


Figure 3: Typical normalized $R_{DS(ON)}$ vs. Junction temperature

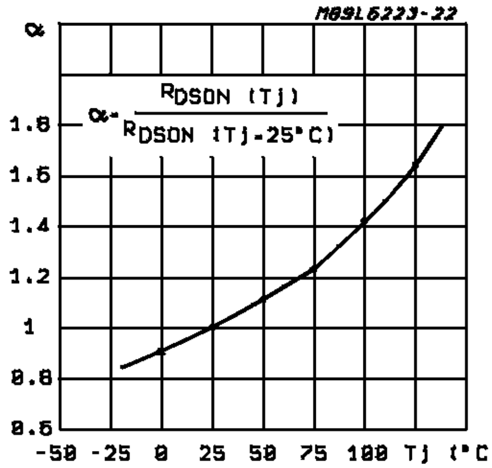


Figure 4: Sense Filter RC Time Constant and PWM Closed Loop control Circuit

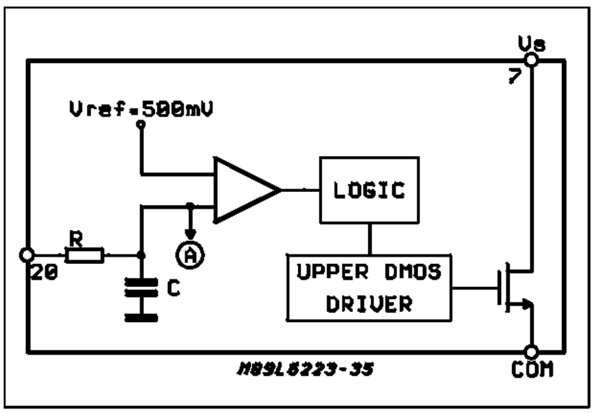


Figure 5: Output Sink Current Delay vs Input Control

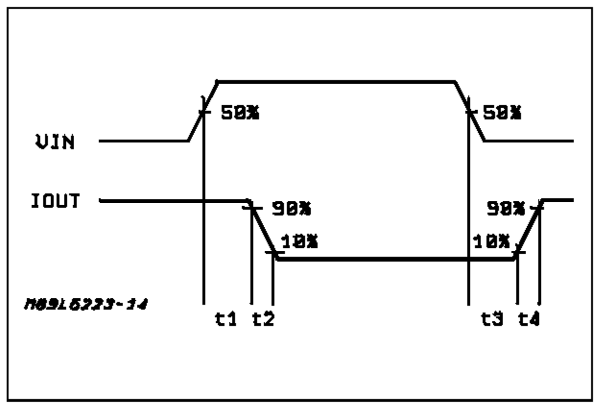
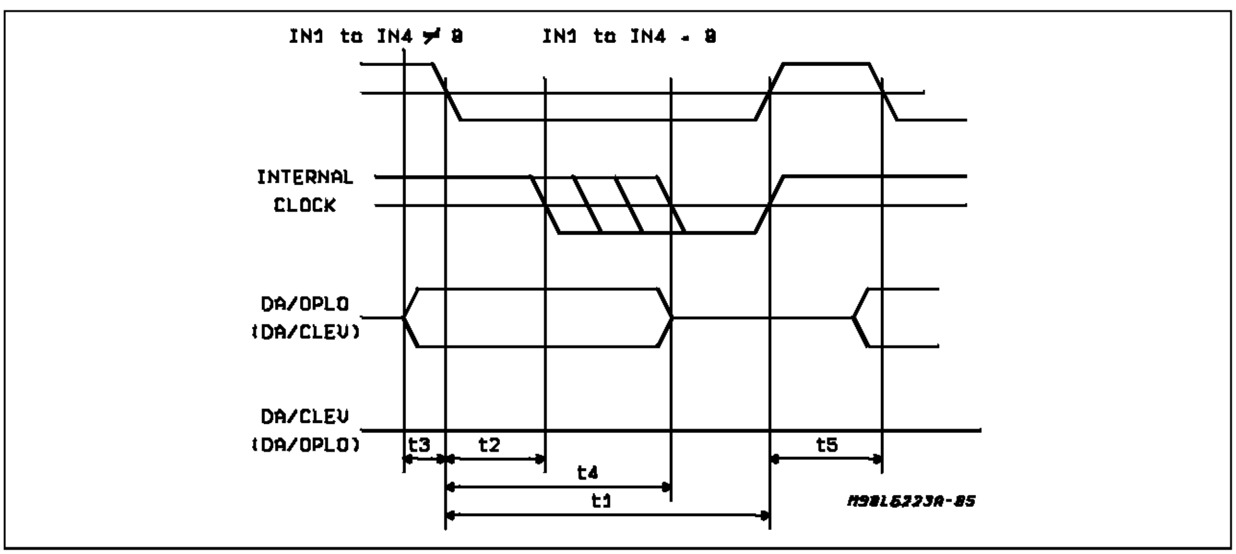


Figure 6: Programming Timing Diagram (see Block Diagram)



BLOCK DIAGRAM DESCRIPTION

Input Logic
Decodes the input signals IN1, IN2, IN3, IN4, DA/OPLO, and DA/CLEV for programming the device and driving the motor. The six inputs are CMOS compatible and can interface directly with a microprocessor.

Predriver Stages
Drive the gates of the five DMOS. They interface the power section with the logic section. The internal inhibit, when activated, disables the power section. The reset initializes the shift register and disables the power section.

6 bit Shift Register
Internal memory which defines the working configuration of the device along with the input signals.

Current Control
When selected with the input DA/OPLO = L (Closed Loop), it will maintain a constant output current level by chopping. The value of the reference voltage, which is compared to the sense voltage, is given by the Ref Block. The chopping frequency depends on bit C4.

Ref Block
Defines the current chopping level according to bits C0 and C1 and the input signals.

Fixed on Time
When selected with DA/OPLO = H, it will define according to bits C2 and C3 the chopping duty cycle for the Open Loop mode. The chopping frequency is fixed.

Oscillator
Provides the clock setting the S/R FLIP-FLOP that turn ON/OFF the upper DMOS (Fig. 22). The higher operative chopping frequency is defined by the external RC network (typically 20KHz). At the phase change a syncronous clock pulse is generated

Reset Logic Block
Generates the reset signal for the logic at power on and disables the outputs. The reset can also be generated externally by setting the RC pin to less that 0.9V.

Thermal Protection
Disables the power section in case of over temperature condition.

Charge Pump
Along with an external bootstrap capacitor connected between the BSTP and COM pins, this block generates the internal over voltage required to drive the upper DMOS on.

Power Output
Driven by the Predriver Stages, it supplies the power for the motor windings.

CIRCUIT OPERATION

The five N DMOS transistors of the output stage drive the unipolar motor windings, controlling the current by chopping. In particular, the four Low side (OUT1, OUT2, OUT3, OUT4) switch the phase configurations, and the High side DMOS (COM) is for chopping control.
For this transistor a charge pump circuit provides its necessary gate drive over voltage.
The microprocessor outputs are interfaced with the L6223A output stages through the input logic block. This block also protects the device from microprocessor output errors and failures from the power section back to the microprocessor outputs. The six digital inputs IN1, IN2, IN3, IN4, DA/CLEV, DA/OPLO, are decoded for motor control and rotation when in ”Operating mode” and used for the internal six Bit memory programming when in ”Programming Mode”.
Table 1 shows the condition that selects these device status. The programming of the internal six bit memory sets operative conditions such as:

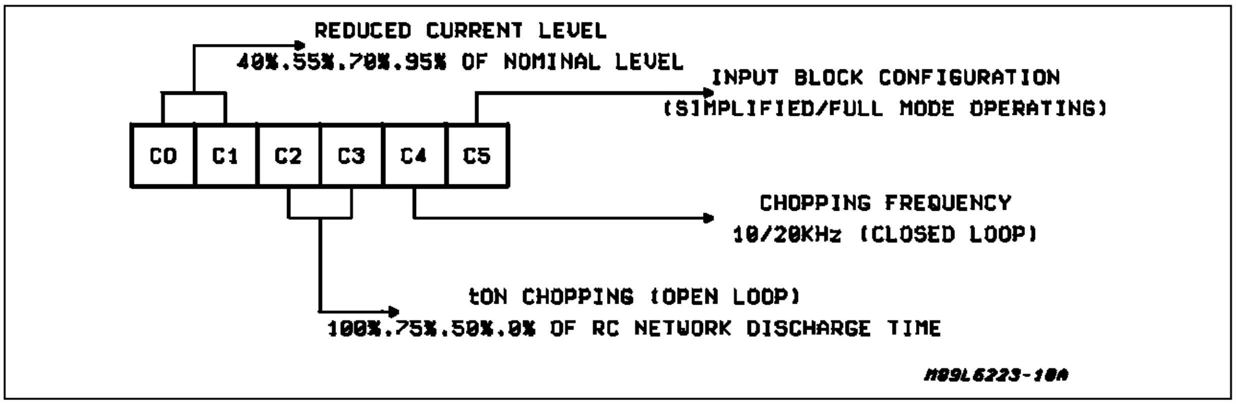
- PWM CURRENT LEVELS
- CHOPPING FREQUENCY
- LOGIC IN/OUT DECONDING

This memory works like a shift register. Each bit is introduced serially by decoding the IN1, IN2, IN3, IN4 low status for the internal clock pulse generation and by the DA/CLEV DA/OPLO, inputs in exor, as data in.
Figure 7 shows the six bit meaning.
In the operating mode two different input drive are possible. In SIMPLIFIED OPERATING MODE the IC needs few logic wire for the motor rotation, but only the full step driving sequence can be performed.

Table 1

Device status	Bit C5	IN1	IN2	IN3	IN4	DA/CLEV	DA/OPLO
Simplified mode operating	L	Phase A Driver	Phase B Driver	Enable	Alternative Current Reduction "LOW"	Current Reductio Active "HIGH"	Open/Closed Loop current control
Full mode operating	H	Phase A	Phase $\overline{A}$ driver	Phase B driver	Phase B driver		
Programming mode	X	L	L	L	L	serial data in	serial data in

Figure 7: Internal Six-Bit Shift Register Bit Functions



CIRCUIT OPERATION (continued)

The FULL OPERATING MODE permits all the driving possibilities. The 4 low side DMOS transistors are drived directly by the 4 inputs IN1, IN2, IN3, IN4 which define directly the phases configuration. The chopping of the motor current can be in open loop or in close loop. When in open loop (fixed on-time block) the DA/OPLO pin is High and the motor current is not controlled but it mostly depends from the bits C2 nd C3. When in close loop the DA/OPLO is Low and the output current is controlled at a constant value defined by the internal reference and by the sensing resistor value. The internal reference depends by the programming bits C0, C1, and by the input configurations. During the power on sequence the reset circuitry prevents current spikes disabling the outputs and by resetting the memory.

Power Section

The basic concept for the current control is explained by examining the winding pair phase A (MA) in Figure 24. With Q5 = ON, Q2 = OFF the current rises until $R_S I_P$ equals the comparator threshold value. The comparator output resets the F/F and Q5 switches off. In this condition the current decay path begins as shown in Figure 25. The current value becomes $I_p/2$, according to the double number of turns interested. In order to reduce the dissipation, Q2 is also driven on. Q5 remains off (PWM off time) up to a new clock pulse sets again the F/F. The winding current behaviour is shown in Figure 26.

Since during PWM off time the current value is half that of the on time and since in a typical application Toff >>Ton, the device dissipation is further reduced.

The five DMOS transistors are connected to the "predriver stages" block, that drives the DMOS gates, and interfaces them to the internal input logic. The "charge pump" provides correct voltage for Q5 UPPER DMOS gate drive by using the external bootstrap capacitor.

Programming Mode

The Programming Mode is defined by the inputs IN1=IN2=IN3=IN4=Low. When in PROGRAMMING MODE the outputs are disabled. The waveform shown in Fig. 8 represents one possible tim-

ing diagram for programming. When the inputs IN1...IN4 are together Low a clock pulse is generated internally which clocks a data bit into the shift register. If the time interval during which all four inputs are Low is less than 0.2µs, no clocks pulse in generated thus preventing undesirable programming. To generate another clock pulse at least one of the four inputs must first go High and then Low again. The first bit is loaded into C0 and after 6 clock pulse it will be in the C5 posistion. Two programming technique are suggested. The first (Fig. 8) uses IN4 in such a way that the power section is disabled the total programming time (the carriage of the 6 programming bits). Fig. 9 shows another technique: the motor driving signals at the inputs IN1...IN4 are interrupted switching IN1...IN4 Low to carry a single bit. This permits the motor to be enabled for the 50% of total programming time. During the motor rotation it's suggested to program the device immediately after the motor phase change: this make neglectable the motor driving discontinuity due to the device programming.

Figure 8: Waveform for programming: the output is disabled during all the programming duration (see Table 4).

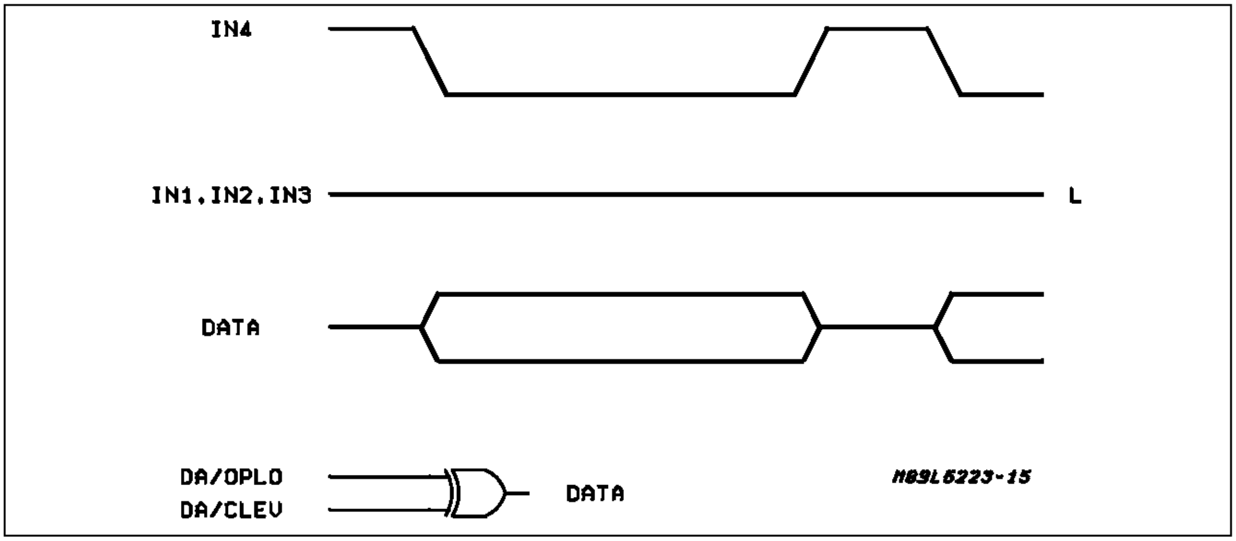
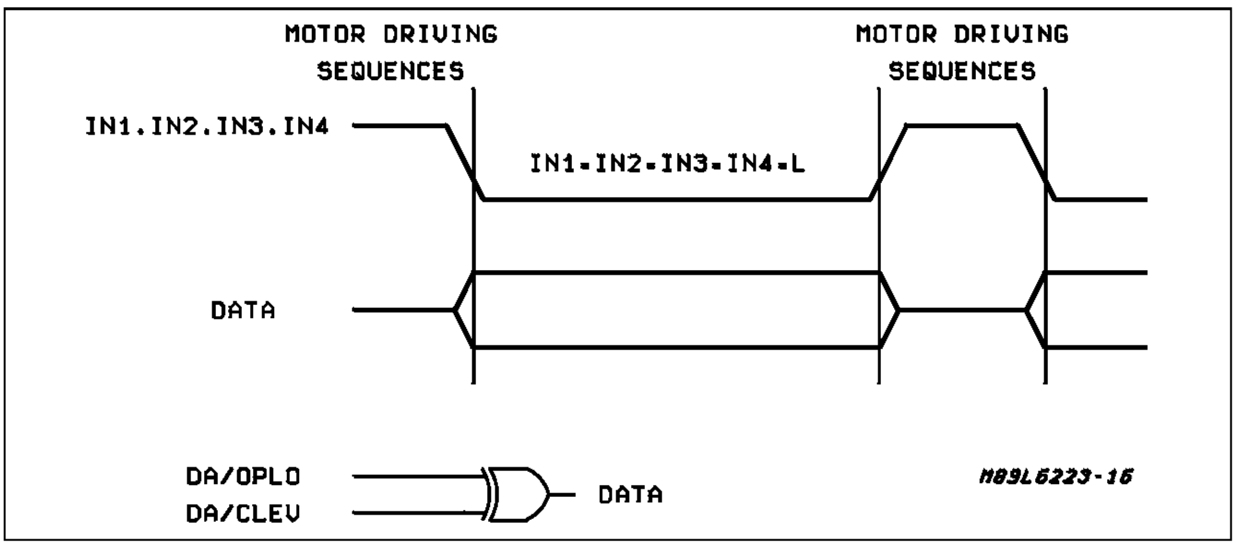


Figure 9: Waveform for programming: the output is disabled only when all four inputs are at the low level.



Operating Mode

The bit C5 defines the two available input configurations.

C5 = H: FULL MODE OPERATING

The digital inputs have the following functions:

- IN1 drives OUT1
- IN2 drives OUT2
- IN3 drives OUT3
- IN4 drives OUT4

The output DMOS is ON when the corrisponding input is low

- DA/CLEV enables the current reduction (see Tab 2)
- DA/OPLO selects the motor current control mode (open or close loop).

Since each input drives one phase of the motor it is possible to work either in Half Step or in Full Step mode. DA/OPLO defines the current control mode as follow:

– DA/OPLO = H open loop
– DA/OPLO = L closed loop

The reduced current level is enabled by the inputs IN1, IN2, IN3, IN4 or by DA/CLEV (Tab. 2). The reduced current value depends from the bits C0, C1 (TAB. 5). The outputs are disabled when the inputs are in a prohibited state (Tab. 4).

C5 = L, SIMPLIFIED MODE OPERATING

When in SIMPLIFIED MODE OPERATING the inputs assume the following functions:

- IN1 drives Phase A
- IN2 drives Phase B
- IN3 ENABLE input (active High)
- IN4 enables the reduced current (Tab. 3)
- DA/CLEV enables the reduced current (Tab. 3)
- DA/OPLO selects the motor current control mode

The SIMPLIFIED MODE OPERATING configuration does not allow the drive of a unipolar motor in Half step.

The signal DA/OPLO functions as in FULL Mode Operation. When the current control is implemented in closed loop, the reduced current level is enabled by the inputs IN4, DA/CLEV (Tab. 3). The current reduction depends from the bits C0, C1 (Tab. 5).

Open/Closed Loop Motor Current Control

The logic input DA/OPLO selects the current control mode as previously seen. When in open loop, the chopping frequency is that one as defined by the external RC network. In open loop are available three different t(ON), depending from the bits C2, C3 (Tab. 6), as a percentage of the RC discharge time $t_{(dis)}$.

When in closed loop two different chopping frequencies are selectable by means of the bit C4 (Tab. 7). The higher is defined by the external RC network. The other one is exactely the half. In closed loop 5 different current levels are available: the nominal current level and four reduced current levels (Tab. 5). The nominal current level is set by an internal reference voltage of 0.5V. The configuration of bits C0, C1 sets the reference voltage to a pecentage of the nominal value.

TRUTH TABLES (L = Low; H = High; X = don't care)

Table 2

IN1	IN2	IN3	IN4	DA/CLEV	C/R*
H	H	X	X	X	H
X	X	H	H	X	H
H	H	H	H	X	H
X	X	X	X	H	H

*) C/R = H, reduced current

Table 3

IN4	DA/CLEV	C/R
L	X	H*
X	H	H*
H	L	L**

*) Reduced current **) Nominal current

Table 4

IN1	IN2	IN3	IN4	Output Stage
L	L	X	X	DISABLED
X	X	L	L	DISABLED

Table 5

C0	C1	Reduced Current Level (*)
L	L	40%
L	H	50%
H	L	70%
H	H	85%

*) Nominal level percentage

Table 6

C2	C3	$t_{(ON)}/t_{(OSC)}$*
L	L	75
L	H	50
H	L	100
H	H	Output Disabled

*) RC discharge time percentage

Table 7

C4	Chopping Frequency
L	20kHz
H	10kHz

L6223A Operating Configuration vs. 6bits Shift Register Programming (External RC network: R = 18kΩ C = 3,3nF)

Nr	SHIFT REGISTER bITS C5	C4	C3	C2	C1	C0	Full/Simpl. Operation Mode	Close Loop Frequency (kHz)	Open Loop $t_{(ON)}$ [%]	Close Loop Current Level [%]
0	0	0	0	0	0	0	S	20	75	40%
1	0	0	0	0	0	1	S	20	75	70%
2	0	0	0	0	1	0	S	20	75	55%
3	0	0	0	0	1	1	S	20	75	85%
4	0	0	0	1	0	0	S	20	100	40%
5	0	0	0	1	0	1	S	20	100	70%
6	0	0	0	1	1	0	S	20	100	55%
7	0	0	0	1	1	1	S	20	100	85%
8	0	0	1	0	0	0	S	20	50	40%
9	0	0	1	0	0	1	S	20	50	70%
10	0	0	1	0	1	0	S	20	50	55%
11	0	0	1	0	1	1	S	20	50	85%
12	0	0	1	1	0	0	S	20	DISABLED	40%
13	0	0	1	1	0	1	S	20	DISABLED	70%
14	0	0	1	1	1	0	S	20	DISABLED	55%
15	0	0	1	1	1	1	S	20	DISABLED	85%
16	0	1	0	0	0	0	S	10	75	40%
17	0	1	0	0	0	1	S	10	75	70%
18	0	1	0	0	1	0	S	10	75	55%
19	0	1	0	0	1	1	S	10	75	85%
20	0	1	0	1	0	0	S	10	100	40%
21	0	1	0	1	0	1	S	10	100	70%
22	0	1	0	1	1	0	S	10	100	55%
23	0	1	0	1	1	1	S	10	100	85%
24	0	1	1	0	0	0	S	10	50	40%
25	0	1	1	0	0	1	S	10	50	70%
26	0	1	1	0	1	0	S	10	50	55%
27	0	1	1	0	1	1	S	10	50	85%
28	0	1	1	1	0	0	S	10	DISABLED	40%
29	0	1	1	1	0	1	S	10	DISABLED	70%
30	0	1	1	1	1	0	S	10	DISABLED	55%
31	0	1	1	1	1	1	S	10	DISABLED	85%
32	1	0	0	0	0	0	F	20	75	40%
33	1	0	0	0	0	1	F	20	75	70%
34	1	0	0	0	1	0	F	20	75	55%
35	1	0	0	0	1	1	F	20	75	85%
36	1	0	0	1	0	0	F	20	100	40%
37	1	0	0	1	0	1	F	20	100	70%
38	1	0	0	1	1	0	F	20	100	55%

L6223A Operating Configuration vs. 6bits Shift Register Programming (Continued)

Nr	SHIFT REGISTER bITS C5	C4	C3	C2	C1	C0	Full/Simpl. Operation Mode	Close Loop Frequency (kHz)	Open Loop $t_{(ON)}$ [%]	Close Loop Current Level [%]
39	1	0	0	1	1	1	F	20	100	85%
40	1	0	1	0	0	0	F	20	50	40%
41	1	0	1	0	0	1	F	20	50	70%
42	1	0	1	0	1	0	F	20	50	55%
43	1	0	1	0	1	1	F	20	50	85%
44	1	0	1	1	0	0	F	20	DISABLED	40%
45	1	0	1	1	0	1	F	20	DISABLED	70%
46	1	0	1	1	1	0	F	20	DISABLED	55%
47	1	0	1	1	1	1	F	20	DISABLED	85%
48	1	1	0	0	0	0	F	10	75	40%
49	1	1	0	0	0	1	F	10	75	70%
50	1	1	0	0	1	0	F	10	75	55%
51	1	1	0	0	1	1	F	10	75	85%
52	1	1	0	1	0	0	F	10	100	40%
53	1	1	0	1	0	1	F	10	100	70%
54	1	1	0	1	1	0	F	10	100	55%
55	1	1	0	1	1	1	F	10	100	85%
56	1	1	1	0	0	0	F	10	50	40%
57	1	1	1	0	0	1	F	10	50	70%
58	1	1	1	0	1	0	F	10	50	55%
59	1	1	1	0	1	1	F	10	50	85%
60	1	1	1	1	0	0	F	10	DISABLED	40%
61	1	1	1	1	0	1	F	10	DISABLED	70%
62	1	1	1	1	1	0	F	10	DISABLED	55%
63	1	1	1	1	1	1	F	10	DISABLED	85%

APPLICATION INFORMATION

Single Device Application

Figure 10 shows a typical Single Device Application. With the shown external RC network, the higher chopping frequency is 20 kHz.

In the figure 11, 12 and 13 are shown the waveforms required to drive the motor in Half/Full Step in FULL MODE OPERATING (FMO) and SIMPLIFIED MODE OPERATING (SMO). The sense resistor defines the total motor current. This means that when two phases are ON, the sense current is two times the phase current. In this case the sense resistor value is $R_S = (V_{ref}/2I_p)$, where V_{ref} is the reference voltage and I_P the phase current. We have supposed that the phase current is of the same intensity in the two phases. When only one phase in ON, the current flowing in the sensing resistor is the phase current: this occurs in half step driving mode. The Figures 14 and 15 show the envelope of the sensing voltage in full and half step respectively.
When current imbalance is not considered, this envelope represents the current level $2I_p$ controlled by the chopping when L6223A is working at 100% of current; in full step this level is constant while in half step two different levels are present (Figure 15). Actually, in full step two phases are always ON, and the chopping current level can be changed only by the controller. In half step when two phases are ON and L6223A is working at nominal current level ($2I_p$), but when only one phase is ON, L6223A selects automatically the reduced current. This level depends upon the programming bits. In Figure 15 the higher level represents the chopping at nominal value (two phases ON), the lower level the chopping at the reduced current (one phase ON). The negative peak shown in the figures represents the fast current recirculation at the phase change.

Fig. 15 shows also what happens when the reduced current level selected is at 70% of the nominal value. The motor torque is proportional to the vectorial sum of the phase currents: it can be seen that the unipolar stepper motor control actuated by L6223A in half step is at constant torque but not at constat current.

Figure 10: Typical Application Circuit using a single device: the max peak current capability is of 1A/phase ($R_S = 0.25\Omega$)

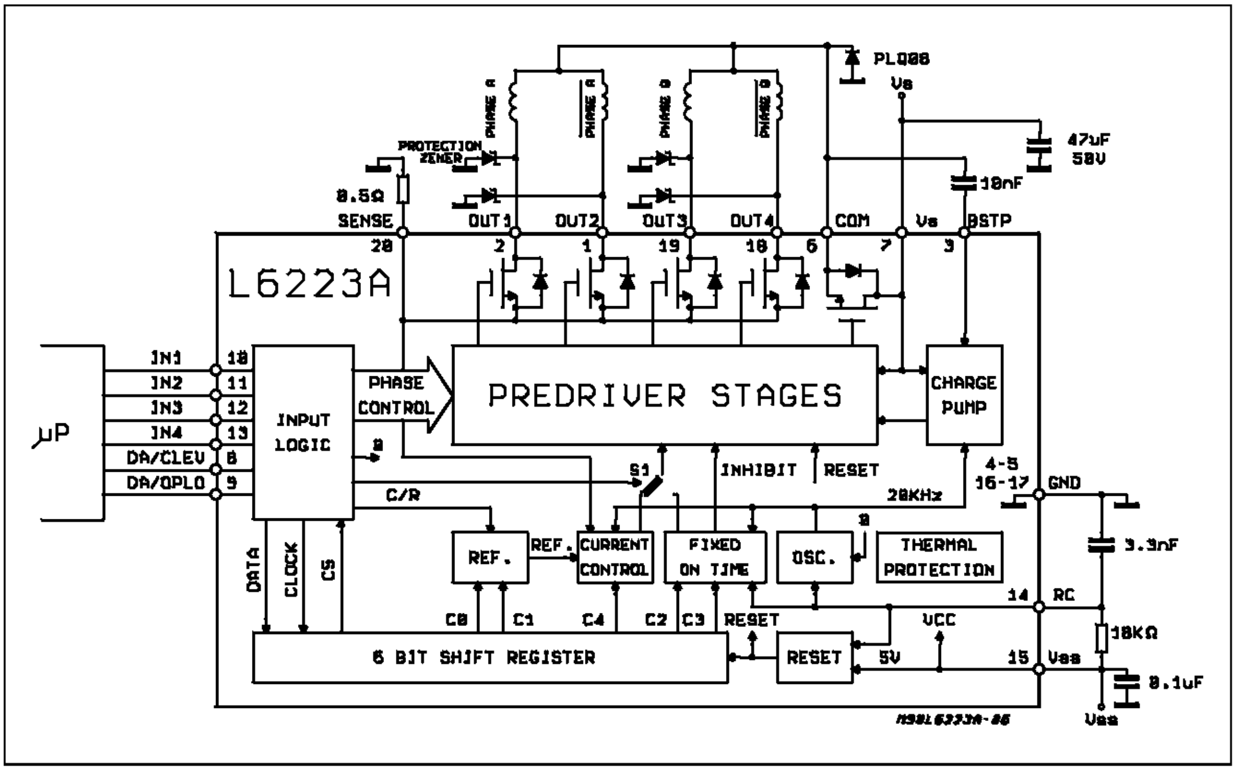


Figure 11: Inputs for Half Step drive, single device FMO.

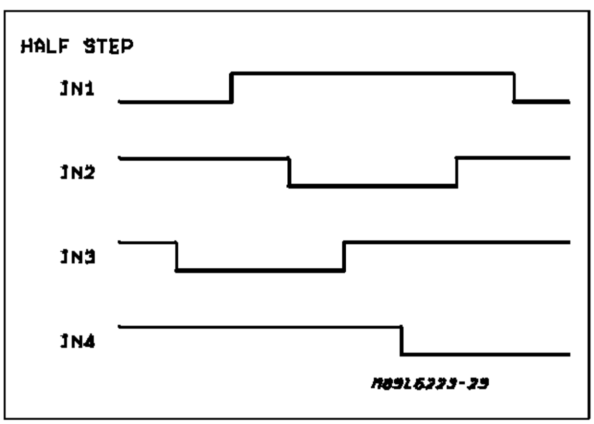


Figure 12: Inputs for Full Step drive, single device FMO.

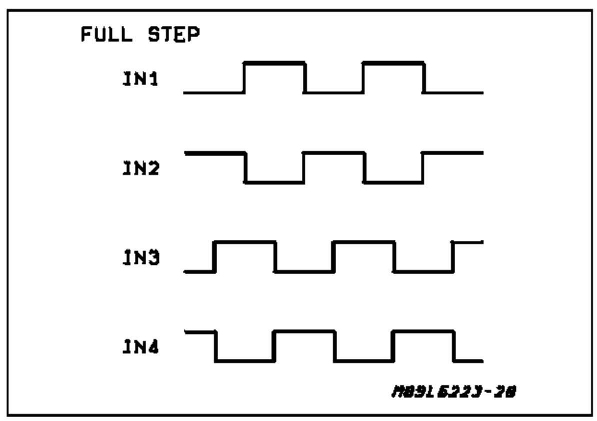


Figure 13: Inputs for Full Step drive single device SMO.

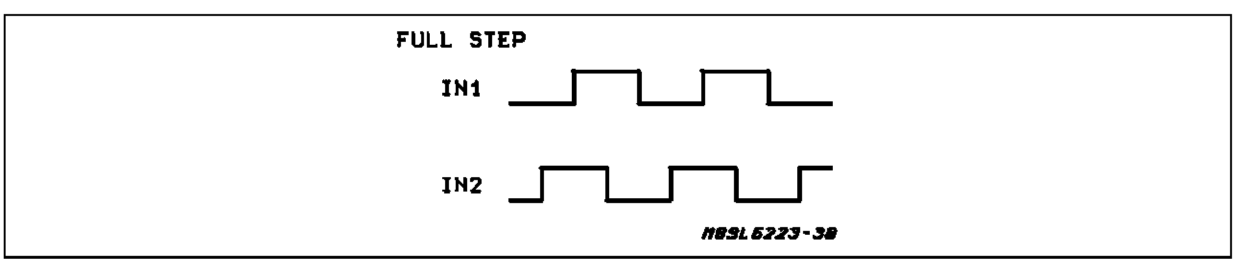


Figure 14: Peak current $2I_p$ crossing the sense resistor R_S in Full step drive. The phase sequence CCW is: AB $\rightarrow$ B$\overline{A}$ $\rightarrow$ $\overline{AB}$ $\rightarrow$ $\overline{B}$A (4 Full Steps, 2 phase ON)

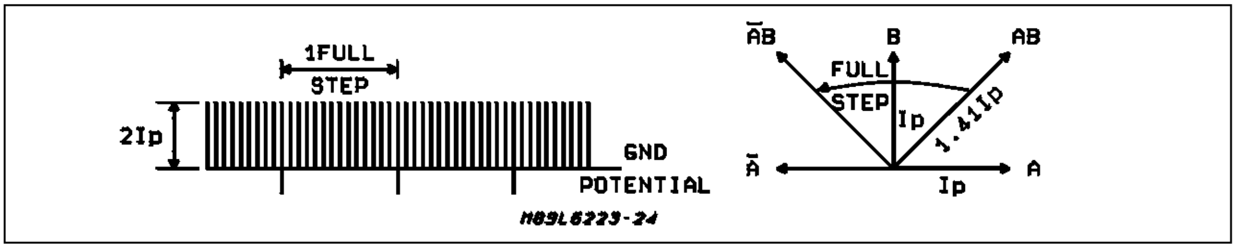


Figure 15: Peak current ($2I_p$/2 phase ON) and reduced peak current ($1.4I_p$/1 phase ON) crossing the sense resistor R_S in Half step drive. The phase sequence is: A $\rightarrow$AB $\rightarrow$ B $\rightarrow$ B$\overline{A}$ $\rightarrow$ $\overline{A}$ $\rightarrow$$\overline{AB}$ $\rightarrow$$\overline{B}$ $\rightarrow$ $\overline{B}$A (8 Half Steps, 1 phase ON and 2 phases ON alternatively)

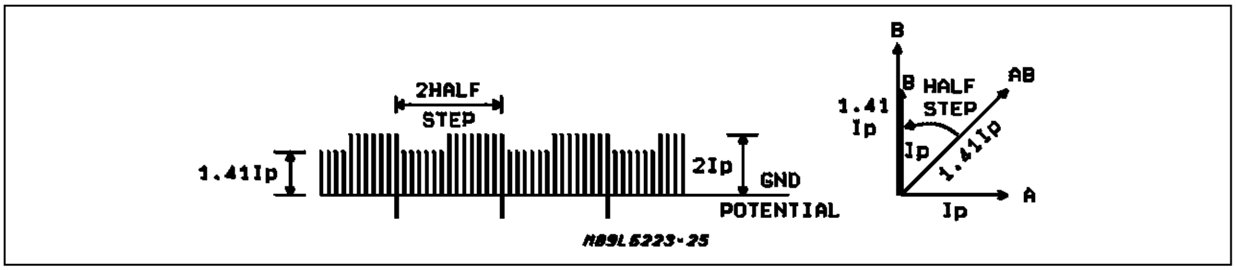
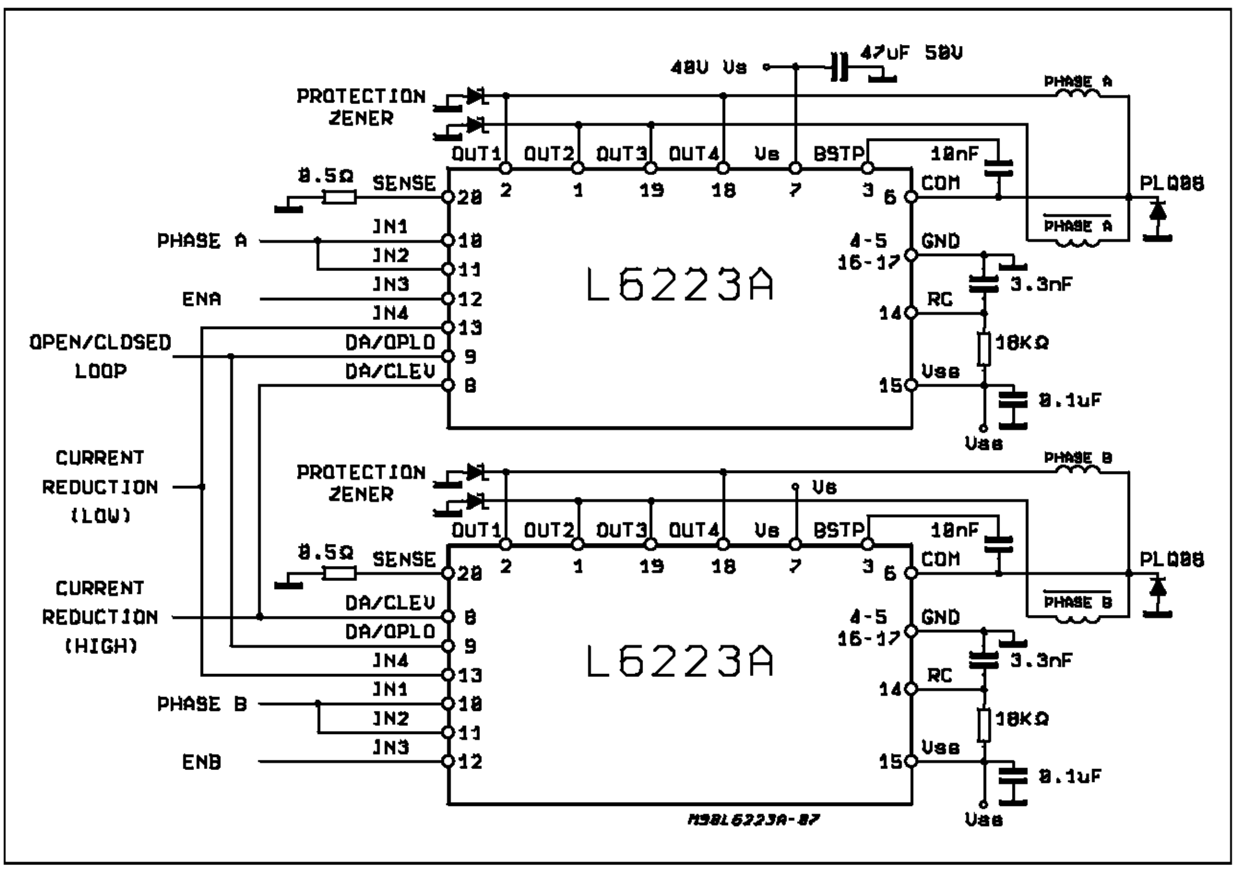


Figure 16: Typical Application Circuit using 2 devices (Paralleled configuration): the max peak current capability is of 2A/phase ($R_S = 0.25\Omega$)



Dual Device Application

Fig. 16 shows how to drive one unipolar stepper motor by means of two L6223A Each device drives one phase of the motor. This permits doubling of the phase current. Since in this configuration each sense resistor controls the phase current (in Single only one sense resistor controls the total motor current), we have: $R_S = (V_{ref}/Ip)$ where V_{ref} is the voltage reference and Ip the phase current in the Dual that is coincident with the chopping current. The configuration in the figure shows the only possible way to parallel two L6223A. The use of another configuration can cause serious demage to the IC during the programming. The waveforms required to drive the motor in half/full step are shown in Fig. 17 and 18: as it can be seen, the two L6223A are in SIMPLIFIED MODE OPERATING configuration. The half step drive can be achieved by driving the inputs IN3 which are ENABLE inputs.

Figure 17: Inputs for Half Step drive dual device SMO.

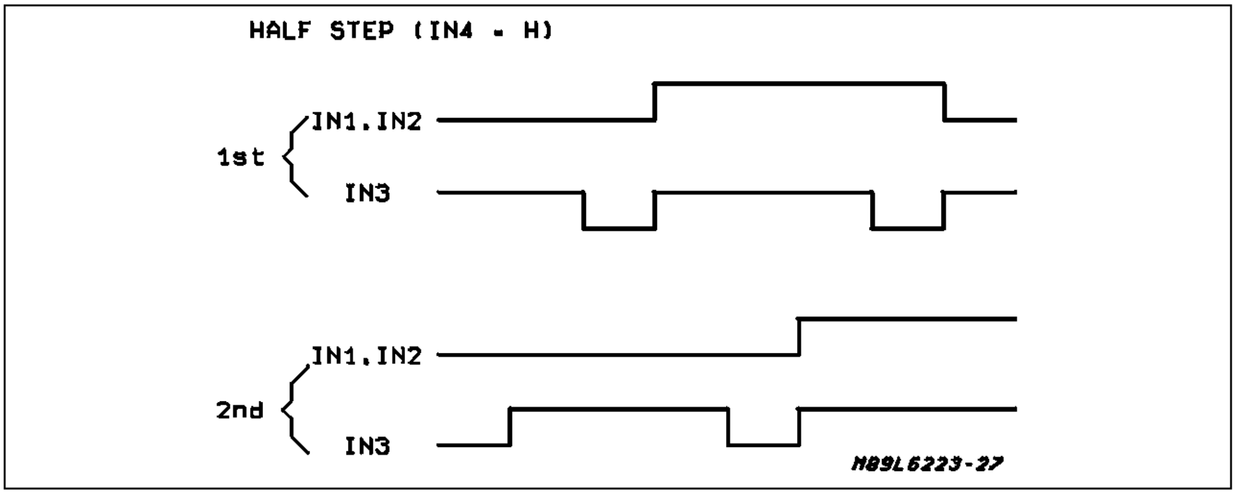
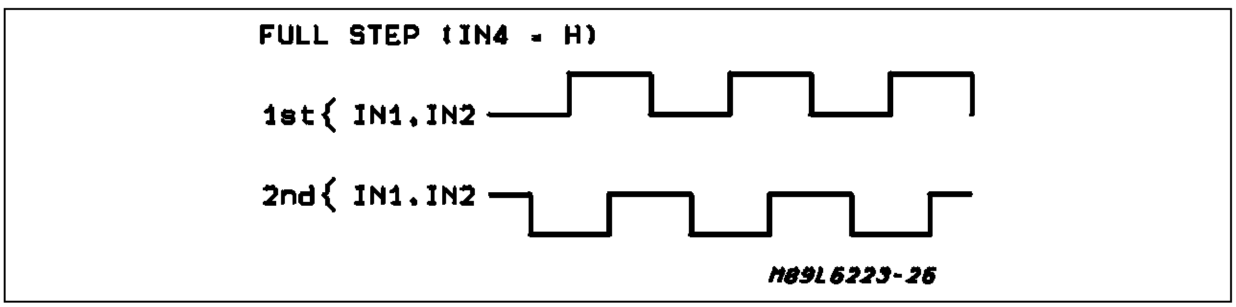


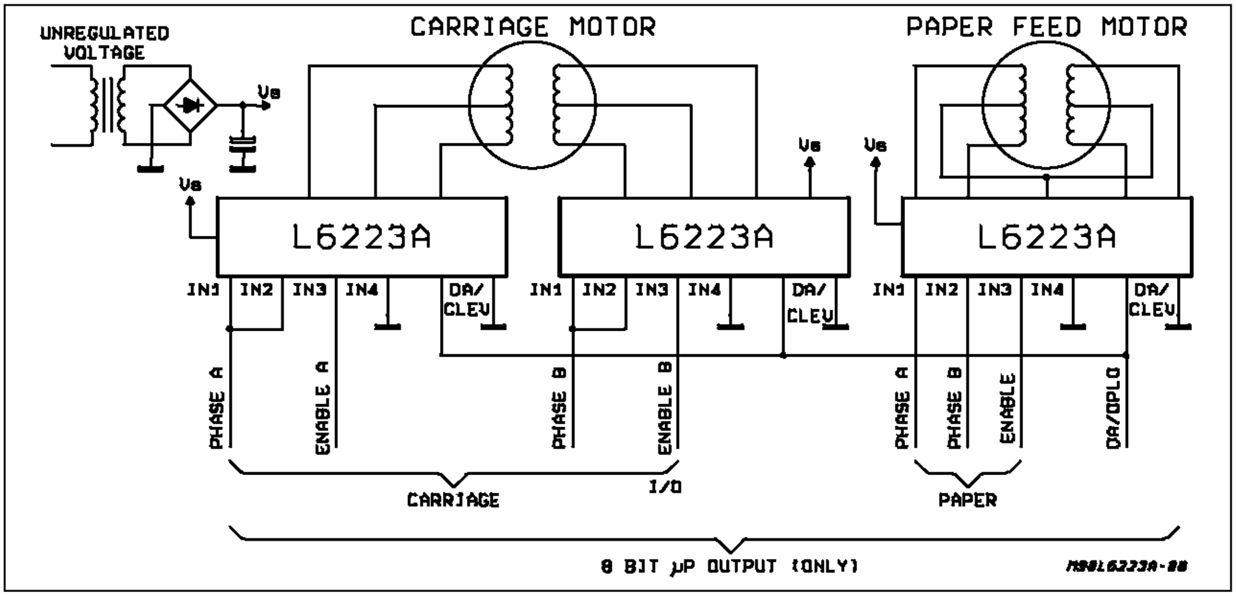
Figure 18: Inputs for Full Step drive single device SMO.



Dot Matrix Printer Motor Driver

Fig. 19 shows how to drive the paper feed and the carriage motors by means of 3 L6223A using a very low wire number. The carriage motor is driven by two paralleled L6223A, the paper feed motor, which requires a lower current, uses one L6223A. The three ICs are working in SIMPLIFIED MODE OPERATING. The inputs IN1-IN2, IN3 are driven as previously seen (Single and Dual Device configuration). The inputs IN4 and DA/CLEV are grounded so that the ICs work in reduced current levels. This means L6223A can select seven current levels through programming: four in closed loop and three in open loop. The input DA/OPLO is used to load the programming data; only the device in PROGRAMMING MODE is programmed. The two paralleled L6223A can deliver up to 2A/phase while the single L6223A, 1A/phase.

Figure 19: Dot Matrix Printer Motor Driver schematic diagram (See also fig. 10, 16).

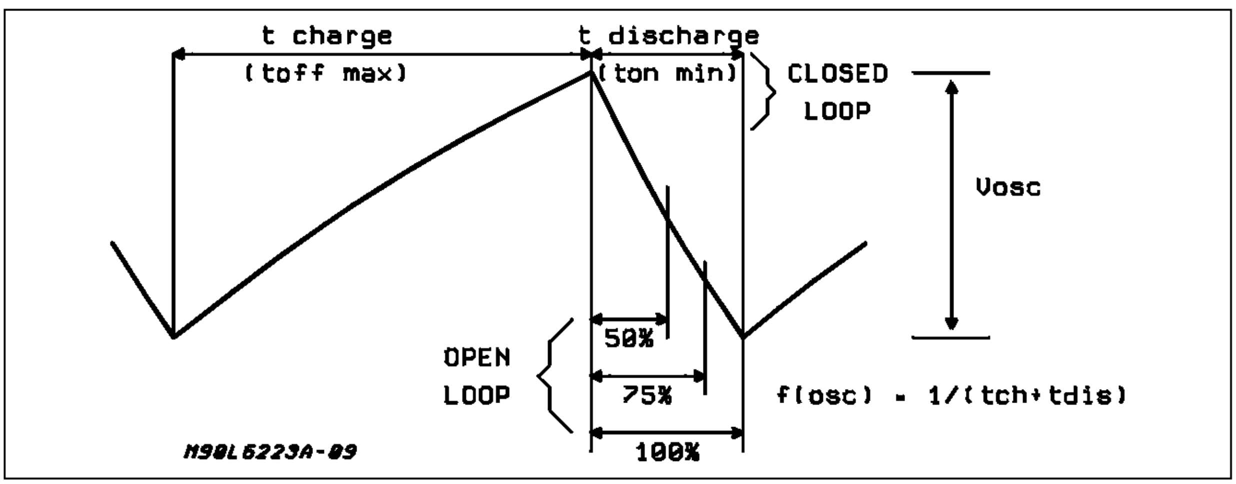


External RC Network (pin 14)

The external RC network provides the higher of the two possible chopping frequencies. The discharge time of the capacitor represents the minimum $t_{(ON)}$ available in closed loop. In open loop it is possible to select a smaller $t_{(ON)}$, (see Fig. 20).

The $t_{(ON)}$ min defines the min current the IC can supply to the motor, as well as the protection "window". This window is necessary to mask the spike generated at the beginning of each chopping period (see Fig. 21a).

Figure 20: Oscillator waveform and timing.



The window must be large enough to mask this spike, without penalizing excessively the min current control. The capacitor C mainly defines the value of the window. The mathematical formulas to calculate the approximate values are:

$f_{(osc)} = 1/(0.84 \bullet RC)$ for $R > 10k\Omega$

$t_{ON(min)} = t_{(window)} = 0.84 \bullet C \bullet R \bullet R_{in}/(R+R_{in})$

for $R_{in} = 1.2k\Omega$

where R_{in} is the resistor internal to the IC for the capacitor discharging.

Figure 21a: Relationship between capacitor discharge of the oscillator, window and sensing voltage

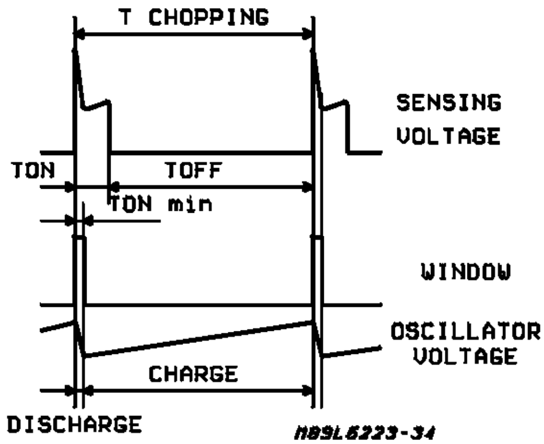
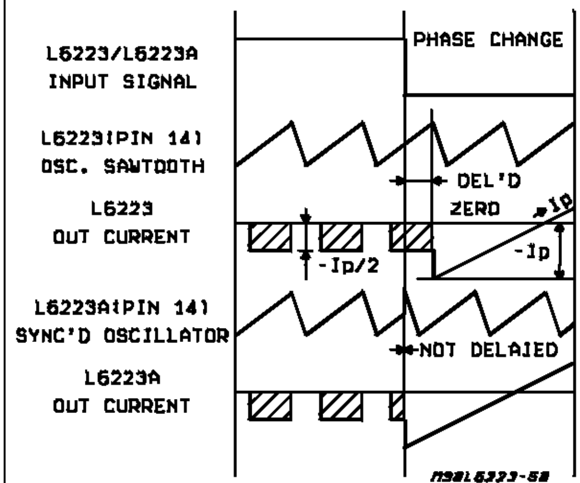


Figure 21b: Oscillator behaviour of the L6223 and of the L6223A (simplified waveforms).

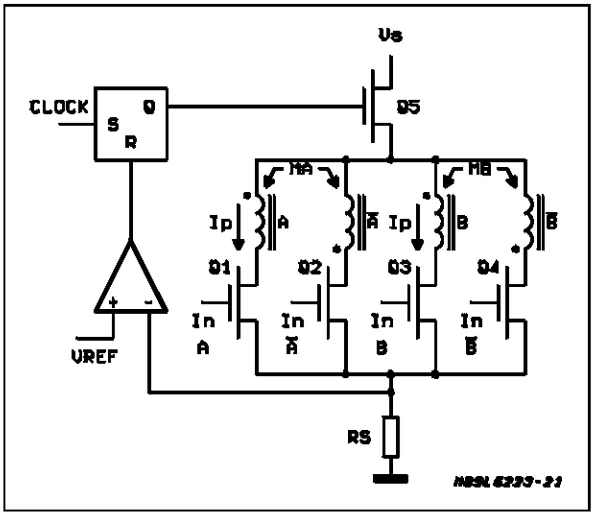


The behaviour of the oscillator at each phase change allows the L6223A to drive high speed unipolar stepper motors.
This is the main functional difference between the L6223A and the L6223 (see fig. 21b).
In the latter, the phase change starts only when the clock pulse sets the F-F (Fig. 22) that is when the capacitor voltage reaches the discharge threshold.
As a result, a variable delay between the leading edge of the input signal and the beginning of the current decay to zero can be expected.
Because of that, driving high speedy stepper motors is produced a noisy beating between chopping frequency and phase change rate.
In the L6223A as soon as the phase change is driven by the inputs, the oscillator voltage Jumps to its top level, a new discharge period is generated and the chopping transistor is switched ON (Q5 in fig. 22). The advantages are a motor phase change synchronous to the driving signal and no beating for whatever rotation speed. By setting pin 14 at a voltage equal or less than Vrs = 0.9V, when the IC is normally supplied and the oscillator is running, the 6 bit shift register is quickly reset and the power outputs are disabled: a delay of 700nsec max must be expected.
The use of this behaviour to reset the device at the turn-on is not allowed; however the reset is automatically provided by the Logic Supply Voltage crossing the threshold of 3.5V (typ.) both at the turn-ON and at the turn-OFF.

Protection

The protection zeners on the outputs protect the IC from overvoltage during chopping and phase change. Actually, at the phase change, the outputs rise to a voltage equal to $V_O = 2V_S + V_m$, where V_S is the power supply and V_m the product of the motor resistance Rm with the peak phase current Ip. Vs is doubled because in the unipolar motor we have two coupled phases connected in series(phase A and $\overline{A}$, B and $\overline{B}$) for each of the two windings of the motor (MA, MB see Fig. 22). The leakage inductance, seen from the outputs of the L6223A, can generate an overvoltage higher than V_O. To protect the IC, the zeners must be able to sustain a power of 400W for 1 microsec and must be able to conduct at a voltage V_z higher than $V_0 = 2V_{s(max)} + V_m$. It's important that during the transition, at the max operating ambient temperature, the zener conduction is guaranteed for a voltage lower than 125V (see Absolute Max Ratings). The ST-BZWO4-85 satisfies this requirement. The diode connected to the common protects this input from the undergounds due to the leakage inductances and/or the imbalancing between the phase currents.

Figure 22: Pover output configuration.



Use of the Programming Mode

A typical application of the L6223A requires driving the motor according to Fig. 23a and Fig. 23b. Starting from $t_0 = t_5$ and continuing until t_1 the motor is kept in stand-by; at time t_1 begins an acceleration period that is completed at time t_3. The motor then is driven at a contant speed until t_4, when the speed is decelerated and is stopped at $t_5 = t_0$ for a new standby period.

During these events the L6223A can be programmed several times for different working modes. The most important parameter is the current through the windings of the stepper: at the time t_0; t_1; t_2; t_3 and t_4 the current can be modified, for example, as it is shown in Fig. 23b. This behaviour allows the best motion control and, at the same time, optimizes efficency of the power output block of the I. C.

But this is not the best in terms of performances by programming: in fact, between t_1 and t_5 the device can be programmed to work in Closed Loop and to chop at half of the RC oscillator frequency during the time t_3 to t_4. In the stand-by condition the I. C. can be programmed to work in Open Loop mode where the current can be fixed by the reduction of the minimum T_{ON} time (75% or 50%) defined by the discharge time of the RC oscillator. Of course in this way the current can be modified by Supply Voltage changes; the same is not possible in Closed Loop operation where the device, in order to keep the windings current constant, modifies the T_{ON} time: wide at low V_S and narrow at high V_S. This is the reason why when the motor is driven at a constant speed (t_3 to t_4) with small current and high Supply Voltage, it could become necessary to program the lower chopping frequency to allow a suitable T_{ON} width otherwise the current of the windings would go out of control.

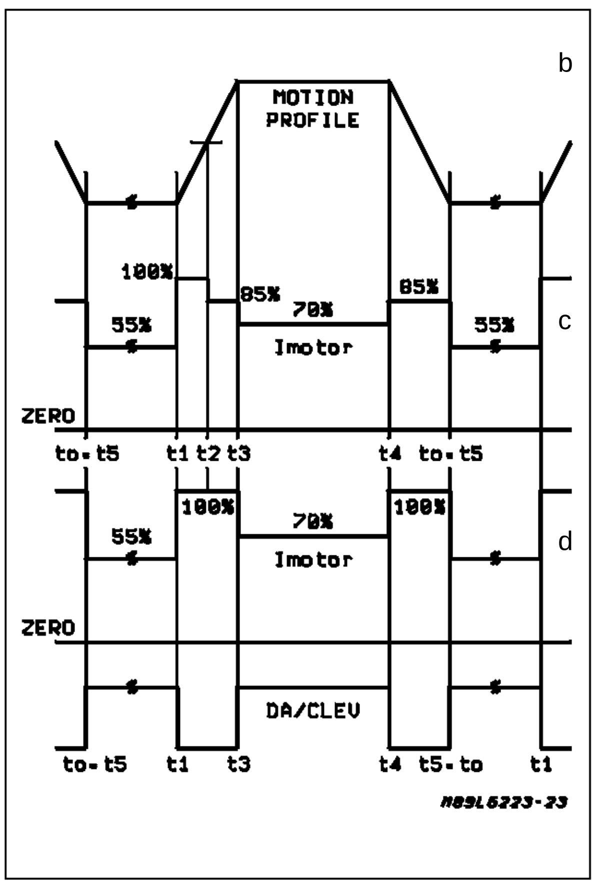
The motion profile, shown in Fig. 23a can be obtained when preferred, with only two program changes actuated while the motor is in stand-by. The current becomes as shown in Fig. 23c. The device can be programmed at $t_0 = t_5$ for I_{motor} = 55% (stand-by) and at t_1 for I_{motor} = 70%: for both the actuations, the DA/CLEV is kept high to allow the program change, while, by keeping it to zero during t_1 - t_3 and t_4 - t_5, the current is automatically select as 100% (Fig. 23d). During t_3 - t_4 the current is reduced according to the percentage programmed at the time t_1.

Power dissipation (Simplified method of calculation).

Here below the Full Step Operating Mode is considered; in addition, the following working conditions have been taken up:

1) Constant speed rotation of the driven unipolar stepper Motor.

Figure 23: a,b) Speed profile and motor current control change for the best efficency of the I.C.a
c,d) Current control change by using DA/CLEV input only, during the stand-by period.



2) Back EMF (BEMF) equal to 80% of its peak during the phase change and equal to 50% of its peak during the chopping period.

3) Constant slope of the current during t_{ON}, t_{OFF} and for power calculation during the phase change (See t_1 in Fig. 27).

4) Current imbalance supposed to be zero.

5) Current ripple during the chopping neglegible. As was previously stated, the current chopping is obtained by means of one PWM Loop that controls the charge time t_{ON} of the inductance of the windings, A and B for example in fig.22.

This time starts each clock pulse and stops when Q5 is switched OFF because of the condition:
$V_{ref} = 2\ R_S I_p$.
A factor 2 is required because the single sensing resistor R_S is crossed by the peak current I_p flowing through each of the two energized windings (A of MA; B of MB).
This configuration can produce an imbalance between the two peak currents because at the phase change the BEMF of one winding (MA) can be out of phase with respect to the BEMF of the other one (MB); in addition, an imbalance may also occur at the phase change when the Power Supply Voltage selected is too low and/or when one motor is driven with too large Lm/Rm ratio.
Nevertheless in most of the applications the dissipated power is not increased and there is no significant change in torque.
During t_{ON} the current Ip, flowing through the phase A (seg. Fig. 24), is defined by V_{ON}
$V_{ON} \cong V_S - R_{tot}\ Ip - BEMF$
where $R_{tot} = R_S + R_m + R_{DSON\ tot}$
in which R_m is the winding resistance of the phase A and $R_{DSON\ tot}$ is the sum of the R_{DSON} of Q1 and Q5: R_m and BEMF are not shown on the Figure 24.
At the end of t_{ON}, the current starts its slow decay and jumps to $I_p/2$ (see Fig. 25) since the total inductance becomes four times L_m (perfect coupling) that is the inductance of the phase A alone.
The recirculation time t_{OFF} is defined by:

$V_{OFF} \cong 2BEMF + I_P\ (R_m + R_{DSONQ1})$

since $R_{DSONQ1} = R_{DSONOQ2}$.
The current through Q1 is shown in Fig. 26: the current ripple is on Ip and $I_P/2$ during t_{ON} and t_{OFF} respectively. It can be obtained the Duty Cycle:
$DC = V_{OFF}\ /\ (2V_{ON} + V_{OFF})$
since $2V_{ON}\ t_{ON} = V_{OFF}\ t_{OFF}$
The slow decay allows a small current ripple as earlier It is considered equal to zero. The current through the phases A and B can be seen in Fig. 27 where the InA and InB signals (see Fig. 22) are shown as well.
These two signals are 90° out of phase with each other and they are 180° out of phase with the corresponding inputs of the IC. In $\overline{A}$ and In $\overline{B}$ are not shown in the Figure.
During the time Tp the motor goes through four steps and the rotation speed V_{rot} (step/sec) can be given by:
$V_{rot} = 4/T_p$.
By considering what was stated above, the following can be applied:

1) Dissipated power by the 4 sink power DMOS (Q1 to Q4).

$$PdL \cong \frac{4\ R_{DSONQ1}\ I_p^2}{T_P}\left[\frac{T_1}{3} + \left(\frac{T_p}{2} + T_1\right)\frac{1 + DC}{2}\right]$$

2) Dissipated power by Q5 (PdH).

$$PdH \cong 4R_{DSONQ5} I_p^2\left[DC + \frac{T_1}{T_p}\left(\frac{4}{3} - 4DC\right)\right]$$

where the phase change duration is:

$$T_1 = -\frac{L_m}{R_{tot}}\ \log_e\left(1 - \frac{2R_{tot}\ I_p}{V_s - 1.6\ BEMF + R_{tot}\ I_P}\right)$$

The chopping produces little power dissipation. It's value can be approximated by:

3) $Pdch \cong 8 \cdot 10^{-3}\ V_s\ I_p$

The sum of 1) + 2) + 3) gives the dissipated power of the output stage. To obtain the total amount of dissipated power it's necessary to include the power dissipation produced by the quiescent currents I_S (from the power stage) and I_{SS} (from the Logical circuits):
$P_{do} = V_S\ I_S + V_{SS}\ I_{SS}$,
considering I_S constat versus V_S. Finally:
$P_{tot} = PdL + PdH + Pdch + Pdo$

Example

Supply Voltage	$V_S = 36V$	
Logic Voltage	$V_{SS} = 5V$	
Peak current (per phase)	$I_p = 0.7A$	
Motor resistance	$R_m = 9\Omega$	at $T_{amb} = 50°C$
Motor inductance	$L_m = 6mH$	
Rotation speed	$V_{rot} = 500$ step/sec (const)	
Peak of the BEMF	BEMF = 1 Vp	
Max ambient temperature	$T_{amb} = 50°C$	
Max junction temperature	$T_j = 125°C$	

From the Electrical Characteristics of the L6223A (Typical value):

Internal Reference Voltage	$V_{ref} = 0.5V$	
Sink DMOS R_{DSON}	R_{DSON} L = 1.2Ω	at Tj = 25°C
Source DMOS R_{DSON}	R_{DSON} H = 0.7Ω	
Power Supply Current	$I_S = 4$ mA	Worst Case
Logic Supply Current	$I_{SS} = 20$ mA	

From Fig. 3 (see pag. 6) the following is obtained:
$\alpha \cong 1.65$ at Tj = 125°C.
The DMOS ON-Resistances become (worst case):

R_{DSON} L = α 1.2 = 2Ω
R_{DSON} H = α 0.7 = 1.15Ω
R_S = 0.36Ω
R_{tot} = 12.5Ω
V_{ON} = 26.24V (During the chopping)
V_{OFF} = 9.7 (During the chopping)
DC = 15.6%
T_p = 8 msec
T_1 = 250µs (During the phase change)
PdL = 1.1W
PdH = 0.4W
Pdch = 0.20W
Pdo = 0.24W
At last:
P_{tot} = 1.94W

The needed thermal resistance between junction and ambient must be equal to:

$$R_{thj\text{-}amb} = \frac{T_{jmasc} - T_{ambmasc}}{P_{tot}} \cong 39°C/W$$

The worst case here considered requires an heatsink of 25°C/W. The calculation of the power dissipation by considering the current imbalance and by simulating a typical motion needed to carry the head of a printer for example, becomes full of difficulties. The use of the Personal Computer is helpful in such a case: few examples are shown from Fig. 28ab until Fig. 31 ab.

Each figure shows the Application Datas and one diagram where the Total Dissipated Power versus the peak of the motor current is plotted.

A max Ambient temperature of 70°C and a max junction temperature of 150°C have been considered for a few applications using one single device and a dual device configuration to drive one

Figure 24: Motor current Ip during t_{ON} (phase MA; Q5 and R_S sre common whit the phase MB).

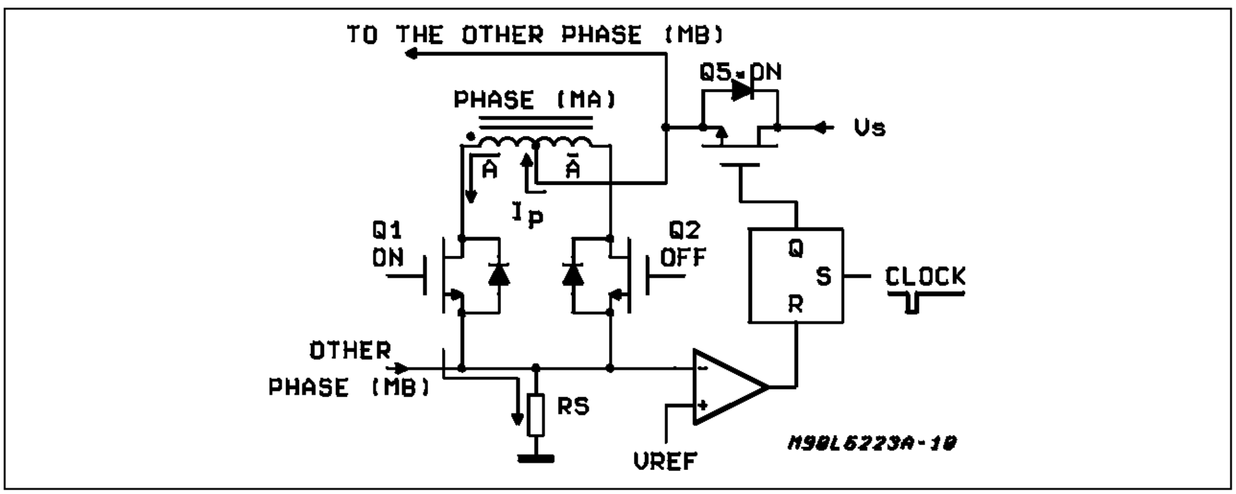
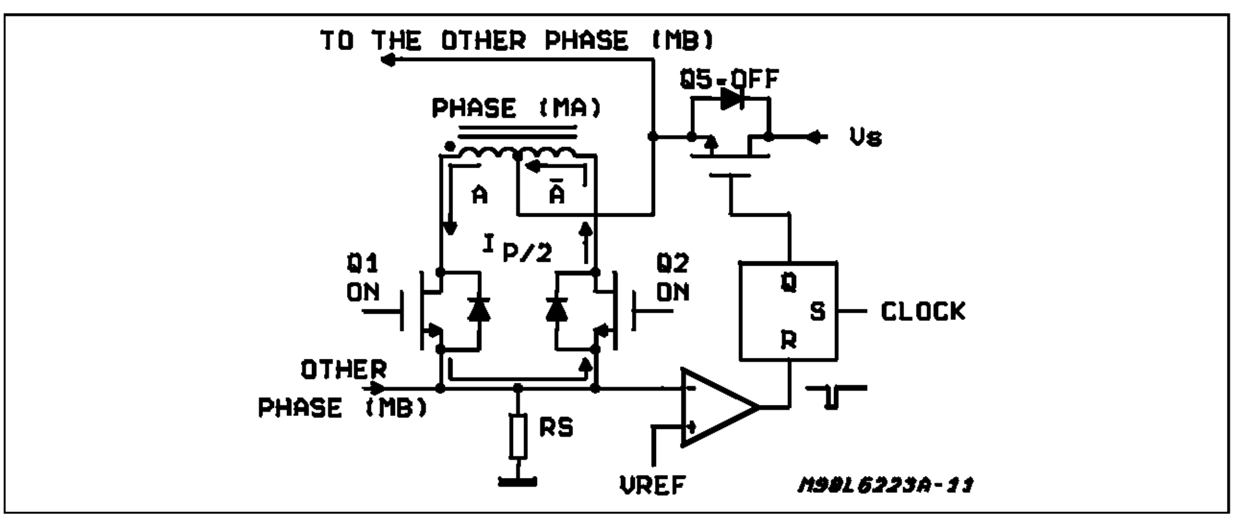


Figure 25: Slow decay of the motor current $I_p/2$ during t_{off} (phase MA).



stepper motor in the Full Step Mode.
The calculations consider three different conditions of heatsinking: the package with minimum dissipating copper area on the p.c.b. ($R_{thj\text{-}amb}$ = 55°C); the copper side of 6 cm^2 ($R_{thj\text{-}amb}$ = 40°C/W - See Fig. 34) and the additional heatsink ($R_{thj\text{-}amb}$ = 30°C/W).

Figure 26: Phase current waveform during chopping: the current decay during t_{OFF} is halved.

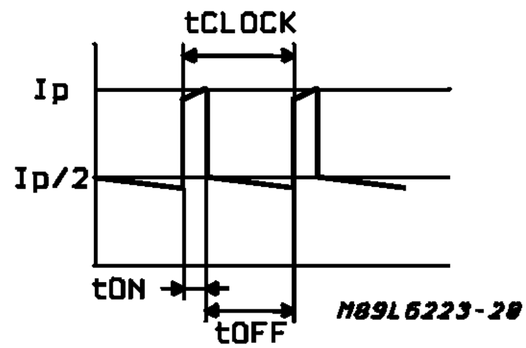


Figure 27: Simplified waveforms of the current through the phase A (winding MA) and through the phase B (winding MB). See also fig.22.

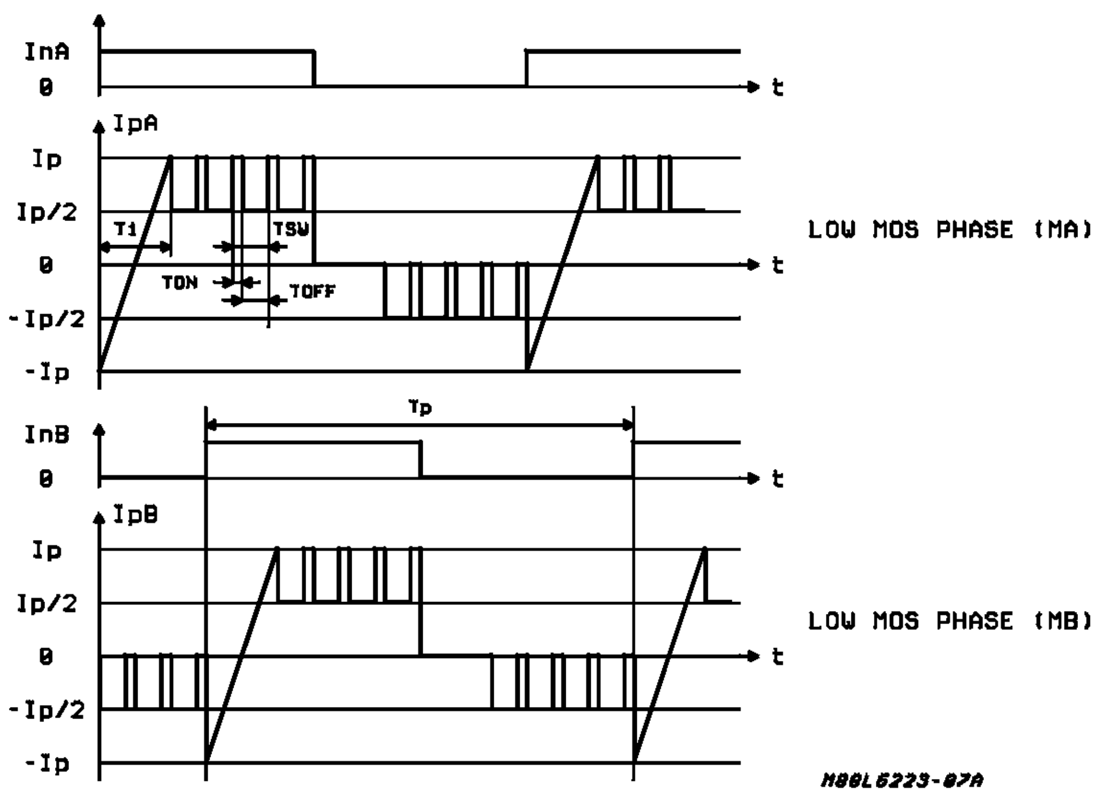


Figure 28a: Single L6223A slow speed, Application Data.

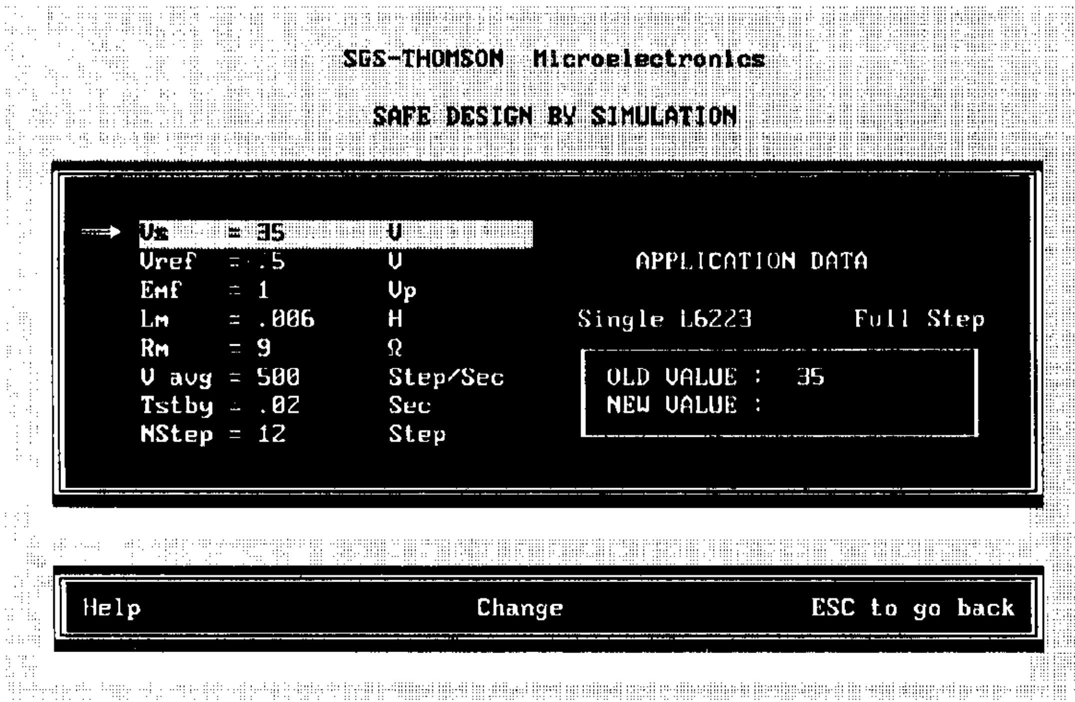
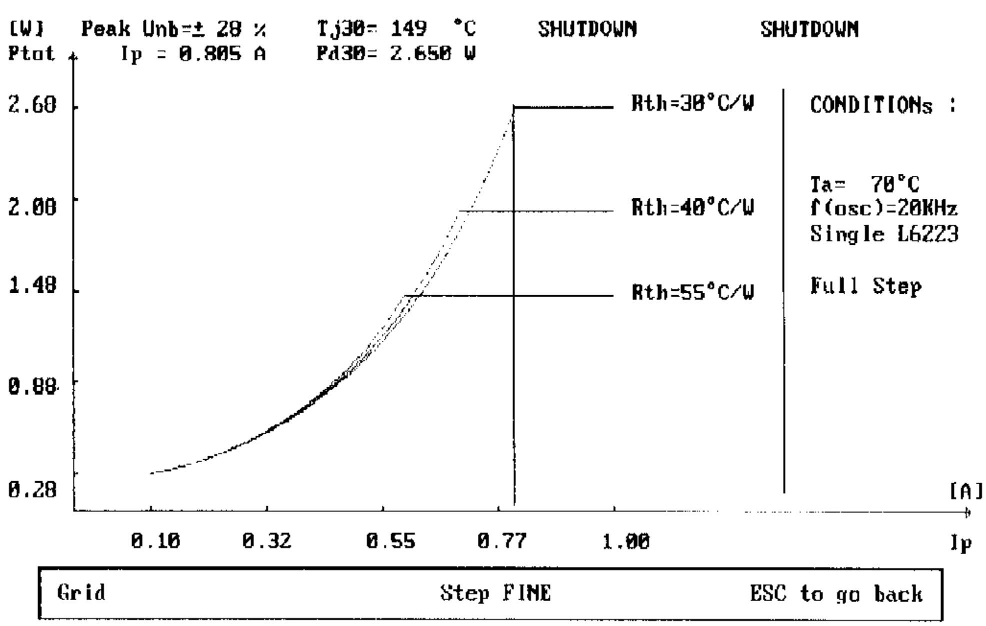


Figure 28b: Total Power Dissipation. The vertical indicator tells us the max value of the current we can supply to the windings (Ip = 0.8A). The peak current corresponding to the flat side of each of the three shown trends is not allowed



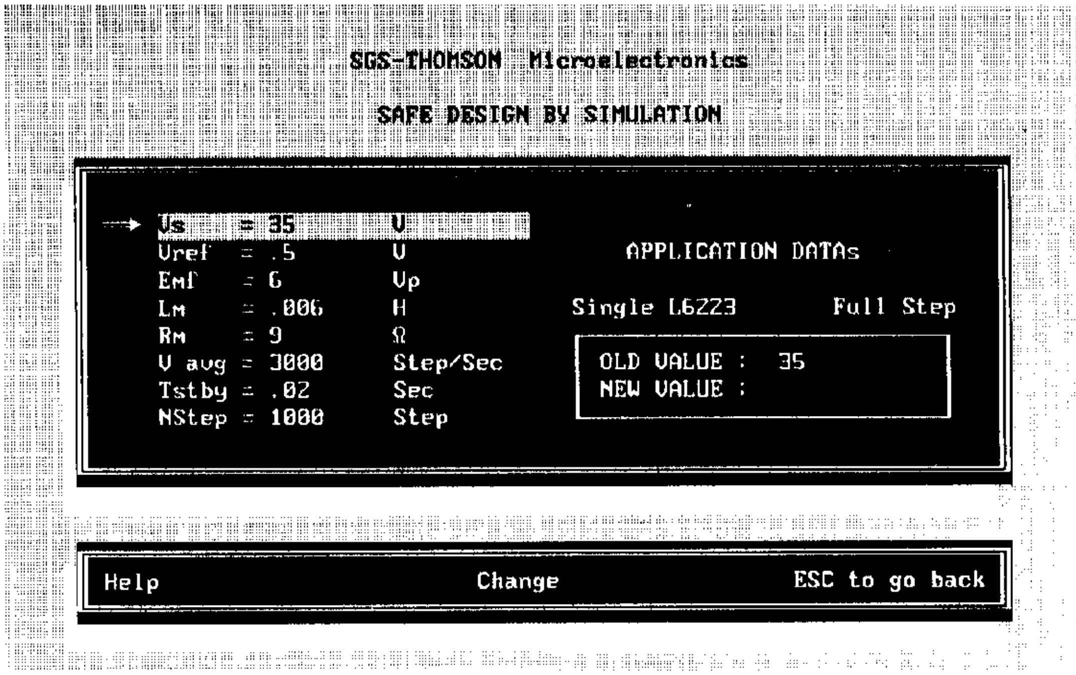


Figure 29a: Single L6223A high speed, Application Data.

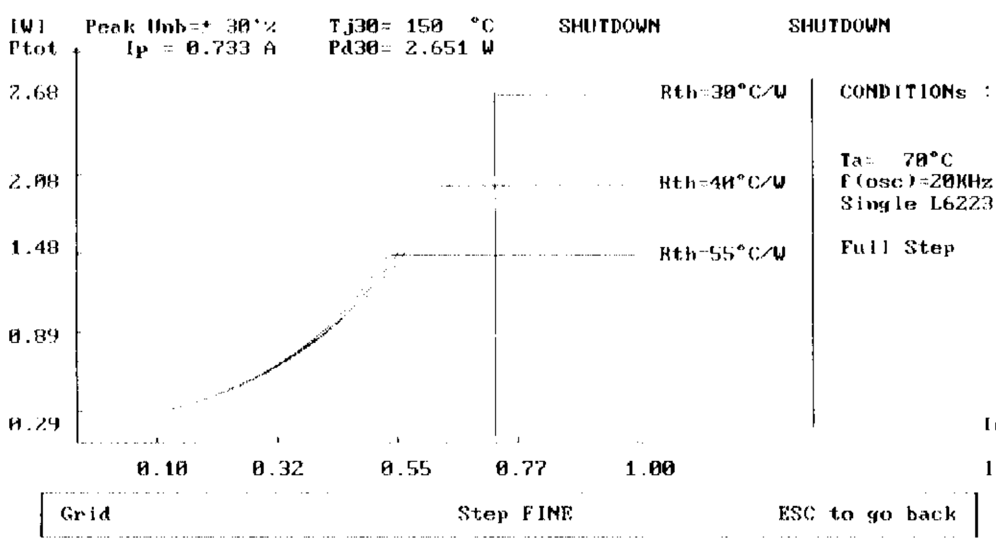


Figure 29b: Total Power Dissipation.

Figure 30a: Dual L6223A slow speed, Application Data.

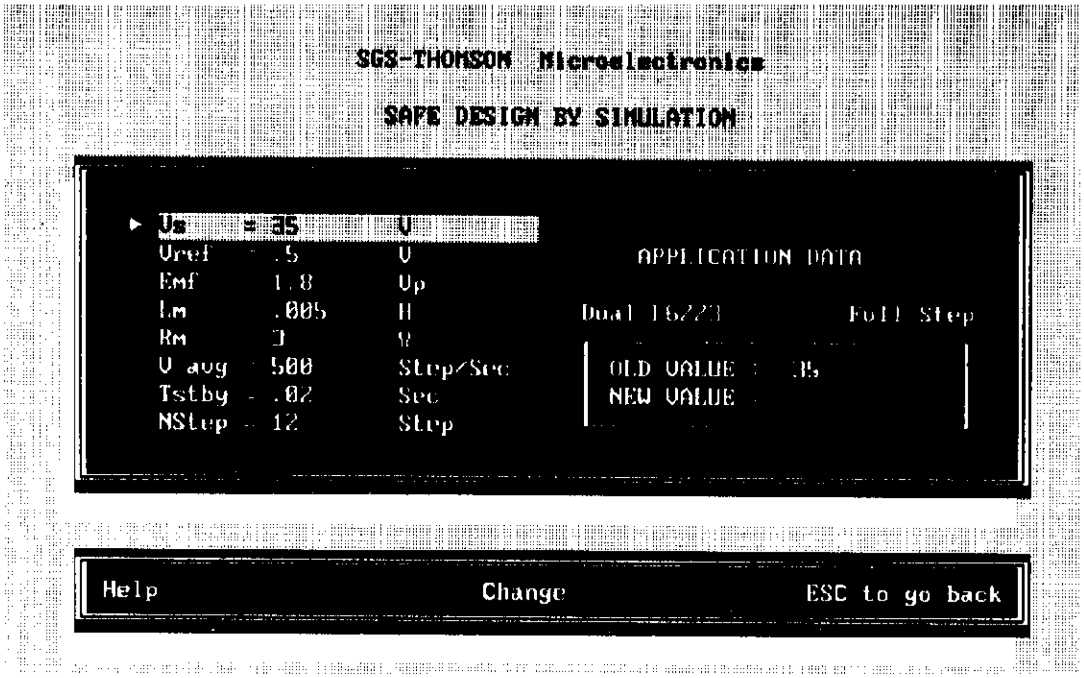


Figure 30b: Total Power Dissipation.

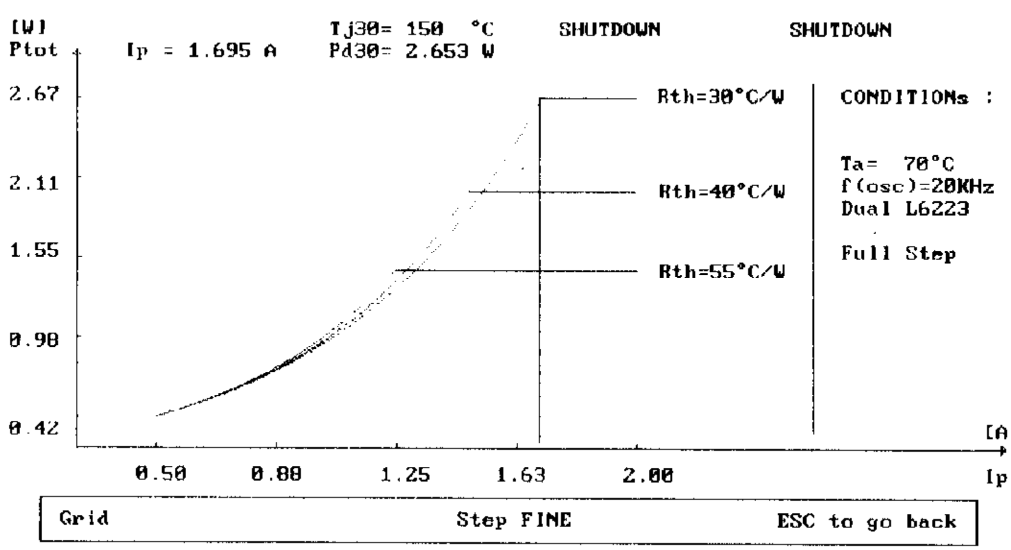


Figure 31a: Dual L6223A high speed, Application Data.

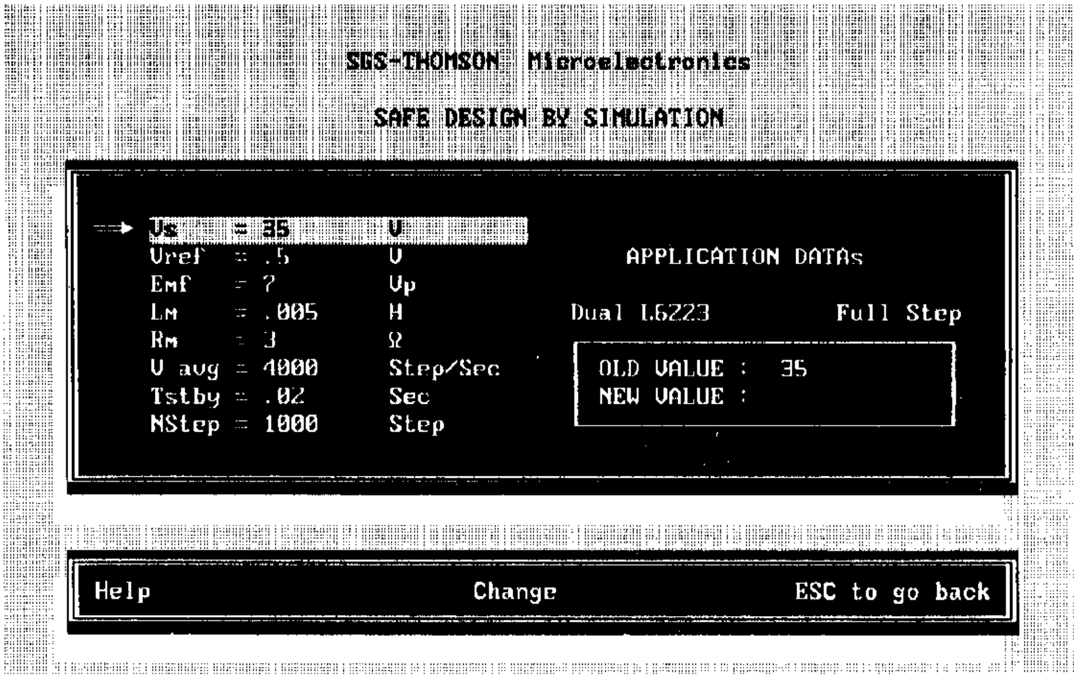
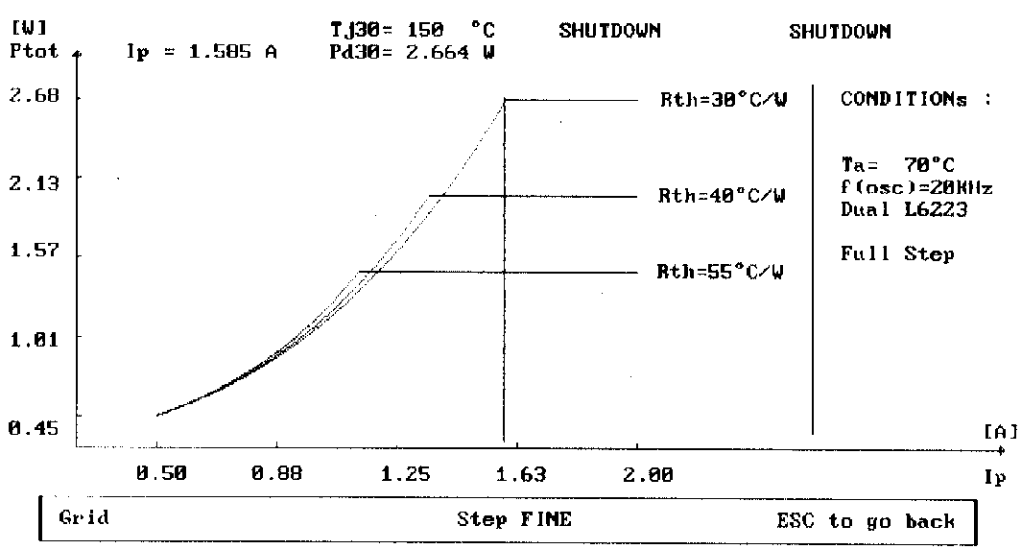


Figure 31b: Total Power Dissipation.



Matching the L6223A with the motor.

For the correct design of the application the following notes must be considered.

* For low motor resistance and high supply voltage the L6223A minimum duty cycle may limit the minimum current at a value higher than requested.
  In this case we suggest to reduce the window protection time changing the RC oscillator network. (See Fig. 21a and External RC Network).
* Only in single device application, for very low motor resistance, a large current imbalance may affect the correct motor rotation. Motor resistance value higher than 7 Ohm are generally recommended for 35V Power Supply.
* The correct motor winding execution is very important for the motor and the L6223A efficiency. A simple test is the measurement of the stray inductance between the central tap and the ends shorted together of each winding. Theoretically the inductance would be zero; values higher than 50µH may show poor motor quality.

Computer Aided Development Board

An improvement in the application development and in system debugging can be obtained by means of the Personal Computer.

Interfacing the appliction with the PC, the motor can be driven directly by this in real time operation. This permits the testing in very short time and a lot of different motion configurations, during application debugging and optimization. Moreover, by paralleling more application boards, an efficient reliability test can be implemented.

The development board designed to drive L6223A in Single and Dual Device configuration is shown in Fig. 32a-b. Fig. 33 is the corresponding electrical circuit. On the board are mounted three L6223A: two for the Dual Device configuration and one for the Single Device. The three connectors J1, J2, J3 allow the application board to be interfaced with the PC and to be paralleled with another one. The remaining connectors provide the interface with the motor and the power and logic supply. The ground area has been sized to act as heatsink (35 micron thickness). When the copper area is not sufficient to dissipate the heat an external heatsink is required.

Figure 32a: L6223A p.c.b. (components side).

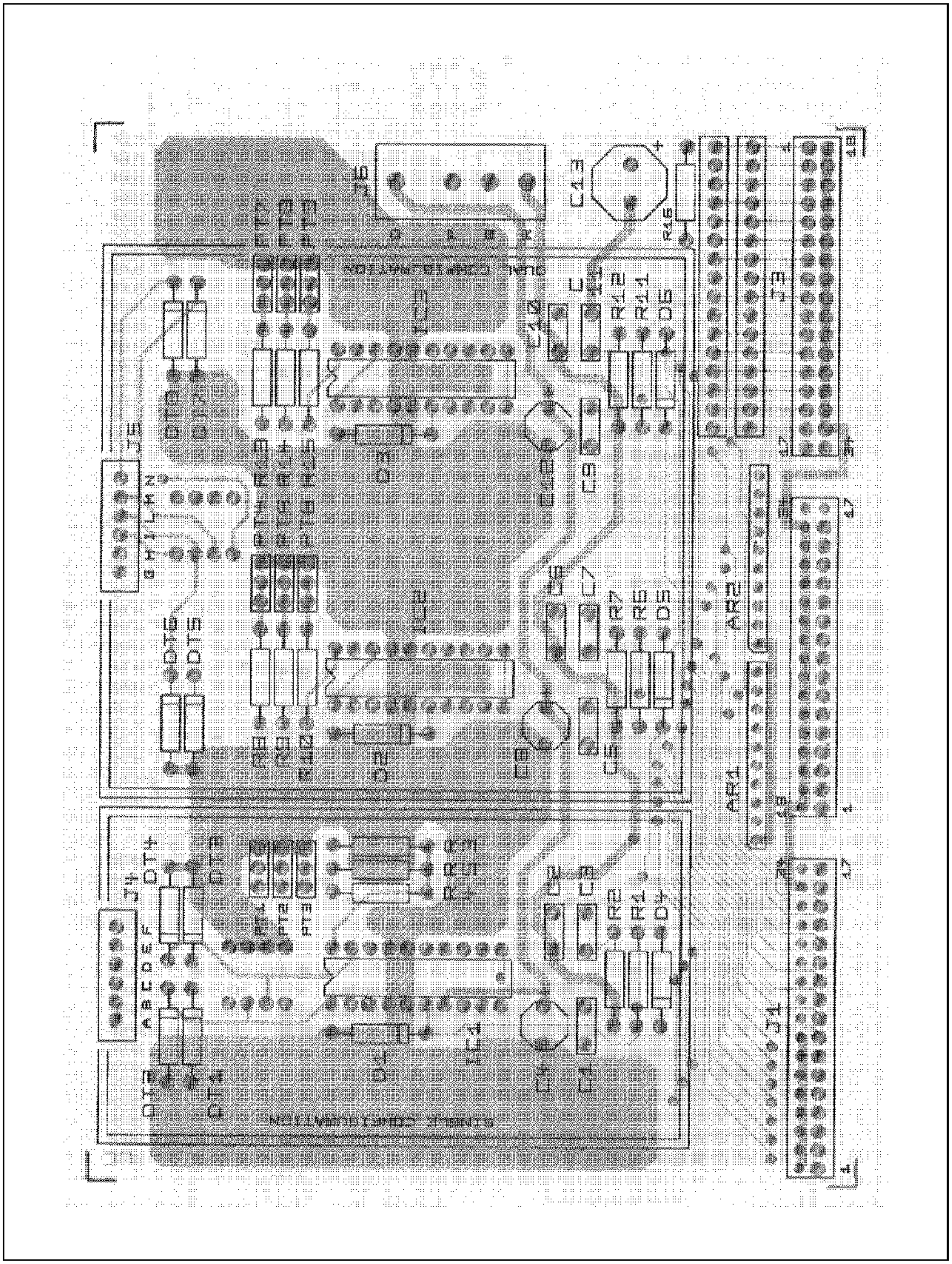


Figure 32b: L6223A p.c.b. (back side).

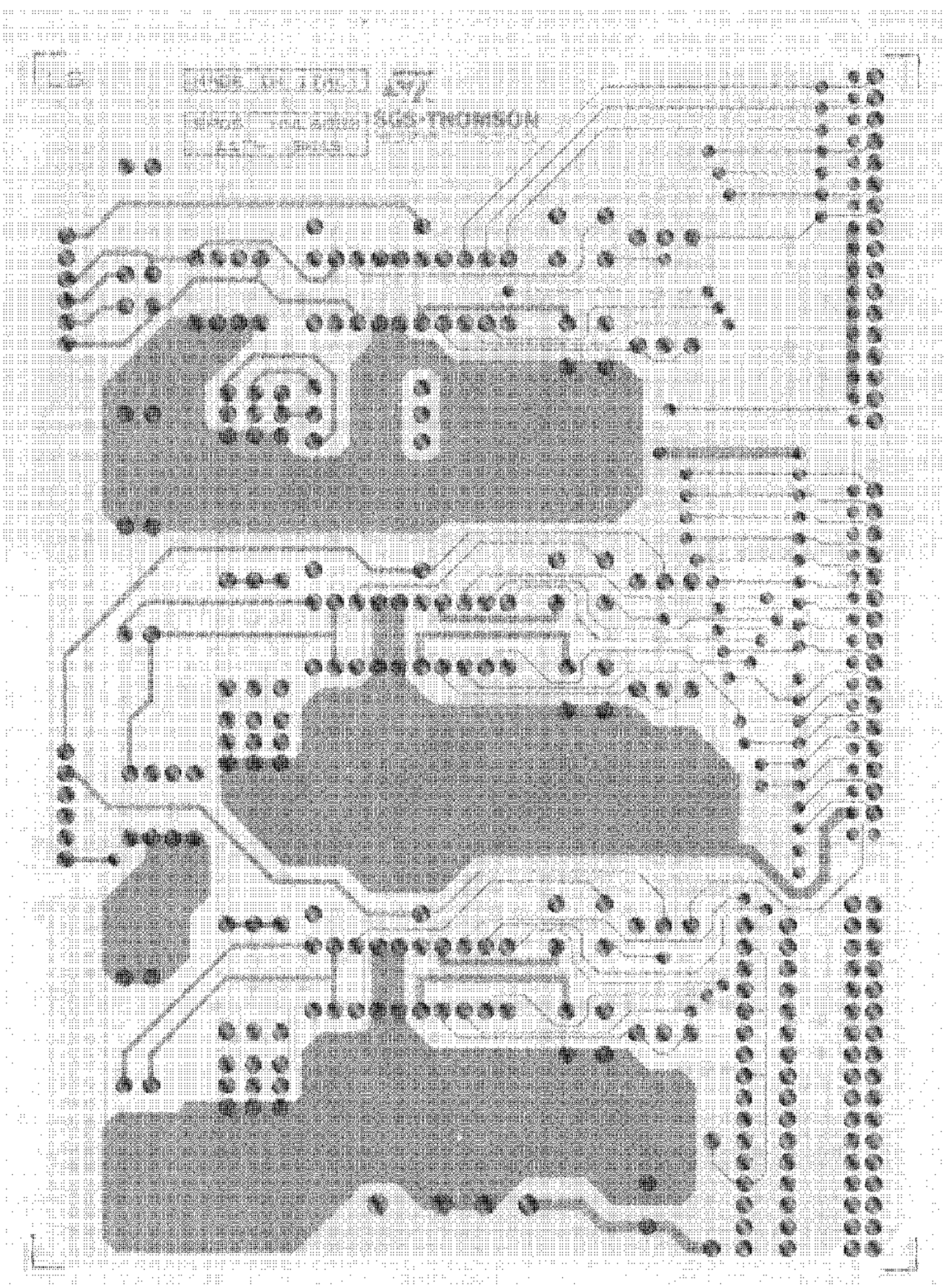


Figure 33: L6223A Development Board schematic diagram.

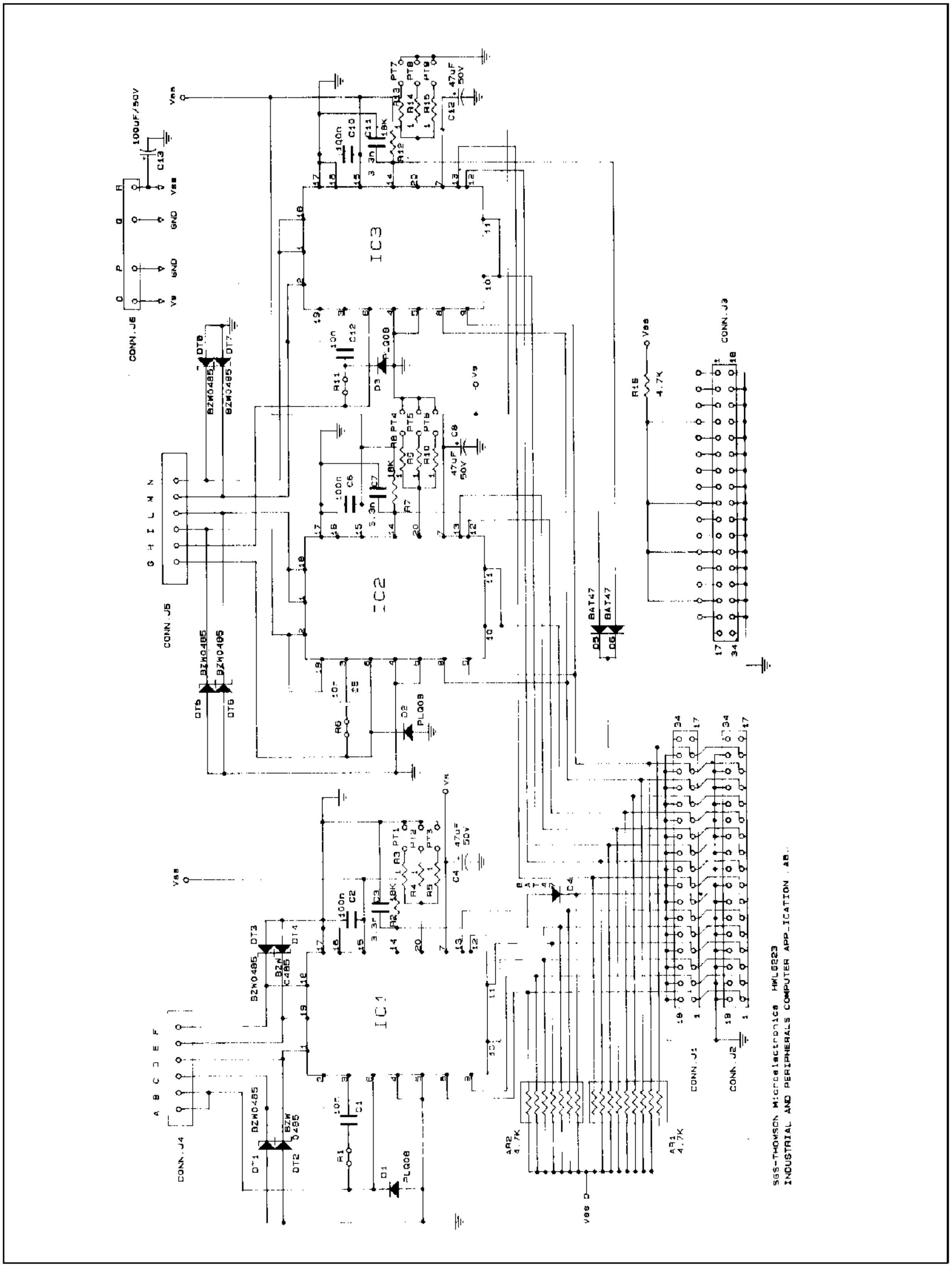


Figure 34: R_{th} with two "on board" square heatsink vs. side l.

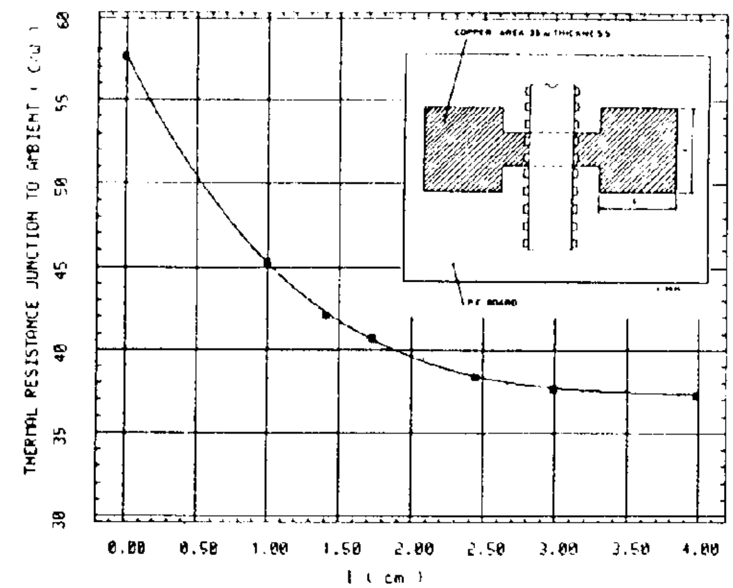
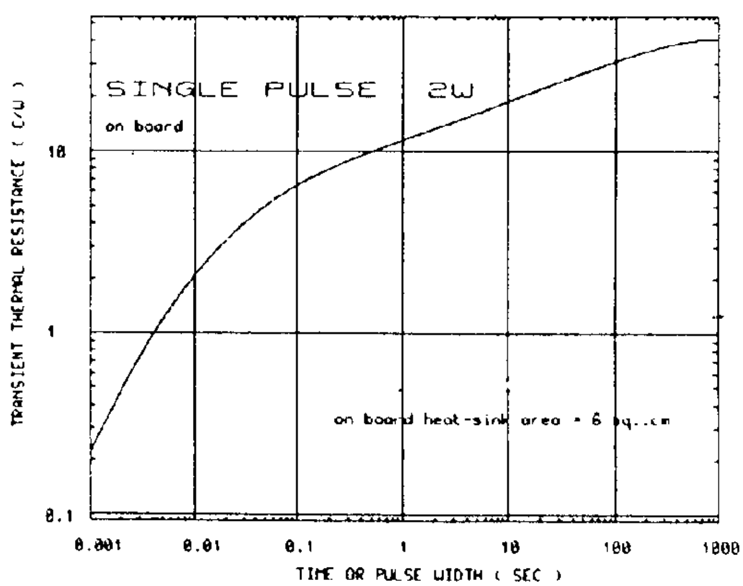


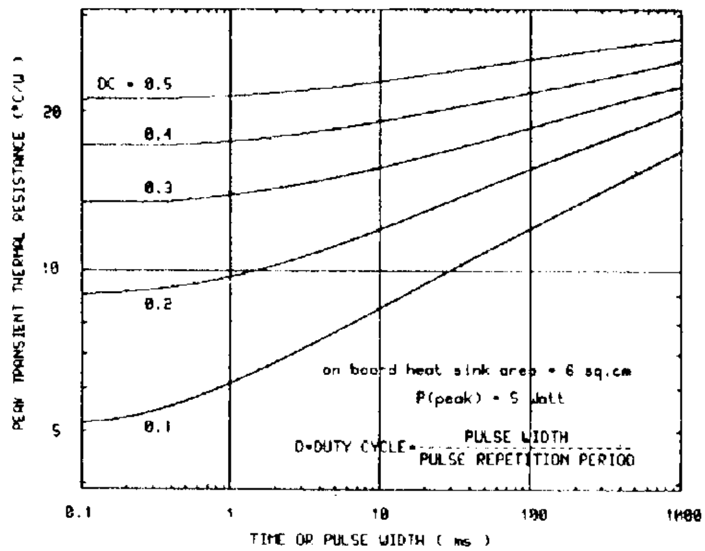
Figure 35: Transient thermal resistance for single pulses



Thermal characteristics.

The p.c.b. copper size needed for a defined thermal resistance between junction and ambient is shown in Fig. 34. Fig. 35 and Fig. 36 are useful to estimate the typical thermal resistance junction to ambient for a single pulse of peak power and for a repetetive peak respectively.

Figure 36: Peak transient Rth pulse width and Duty Cycle.



Notes on the p.c.b. design.

We recommend to observe the following layout rules to avoid application problems associated with ground loops and anomalous recirculation currents. The by-pass capacitors for the power and logic supply must to be kept as close to the IC as possible.

It's important to separate on the PCB board the logic and the power grounds avoiding that grounds traces of the logic signals cross the ground traces of the power signals. The starpoint grounding, the point of the board in which the logic ground meets the power ground, should be kept far enough away from where the power ground traces terminate to ground (sense resistors and protection zener diodes traces). This avoids interference with the logic signals. Because the IC uses the board as a heatsink the dissipating copper area must be sized in accordance with the required value of $R_{thj-amb}$. It's important to provide a good filter for the logic supply, especially for the resistor of the oscillator network. In addition, the capacitor ground of the RC network must be as clean as possible. When the ground is used also to heatsink, it is helpful to use either a polistyrin capacitor or one with a low temperature coefficient. The value of the bootstrap capacitor is not a critical parameter, nevertheless the use of a capacitor of 10nF±20% is recommended. A non-inductive resistor is the best way to implement the sensing, but when that is not possible, more metalfilm resistors of the same value can be paralleled.

POWERDIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

